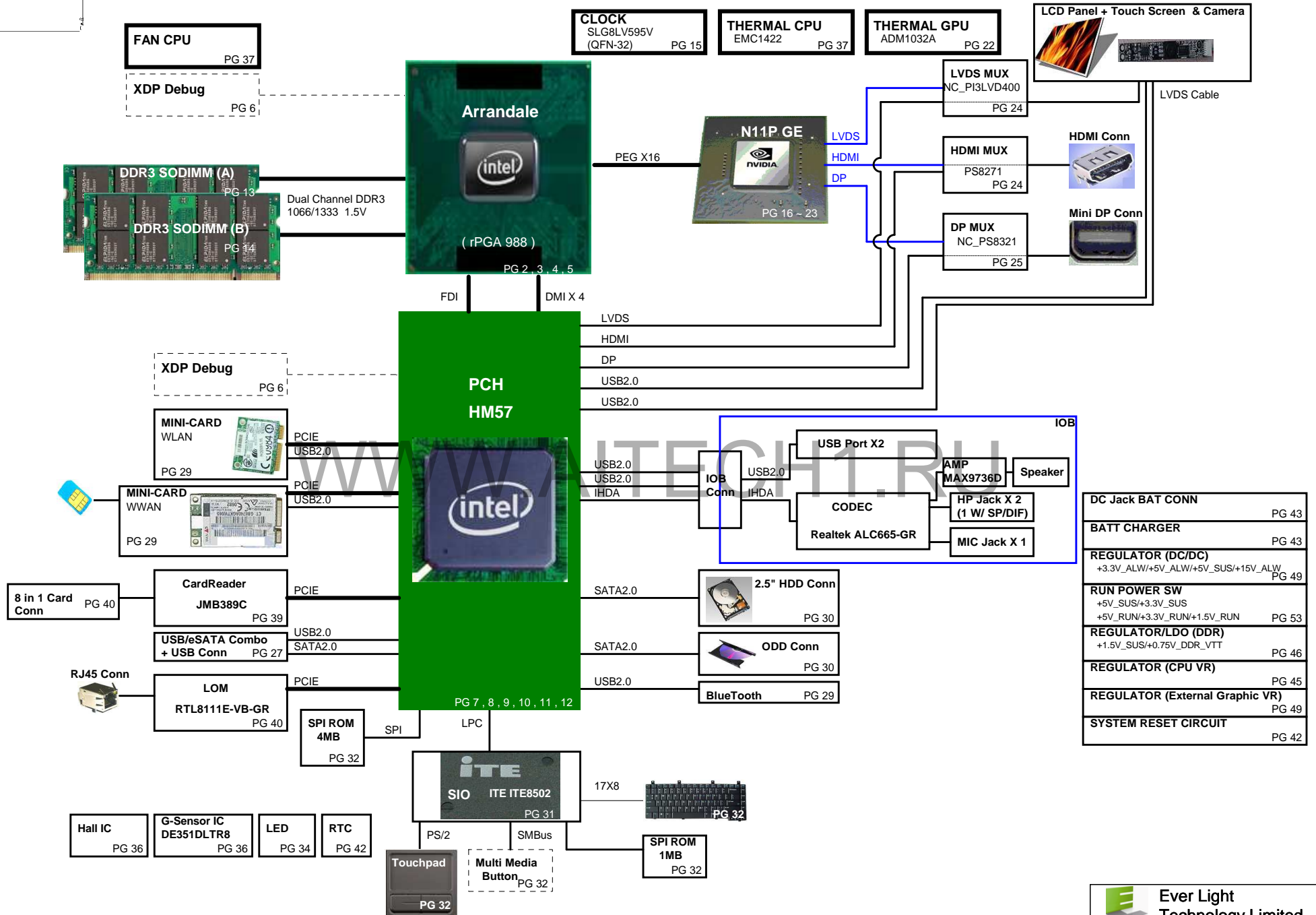
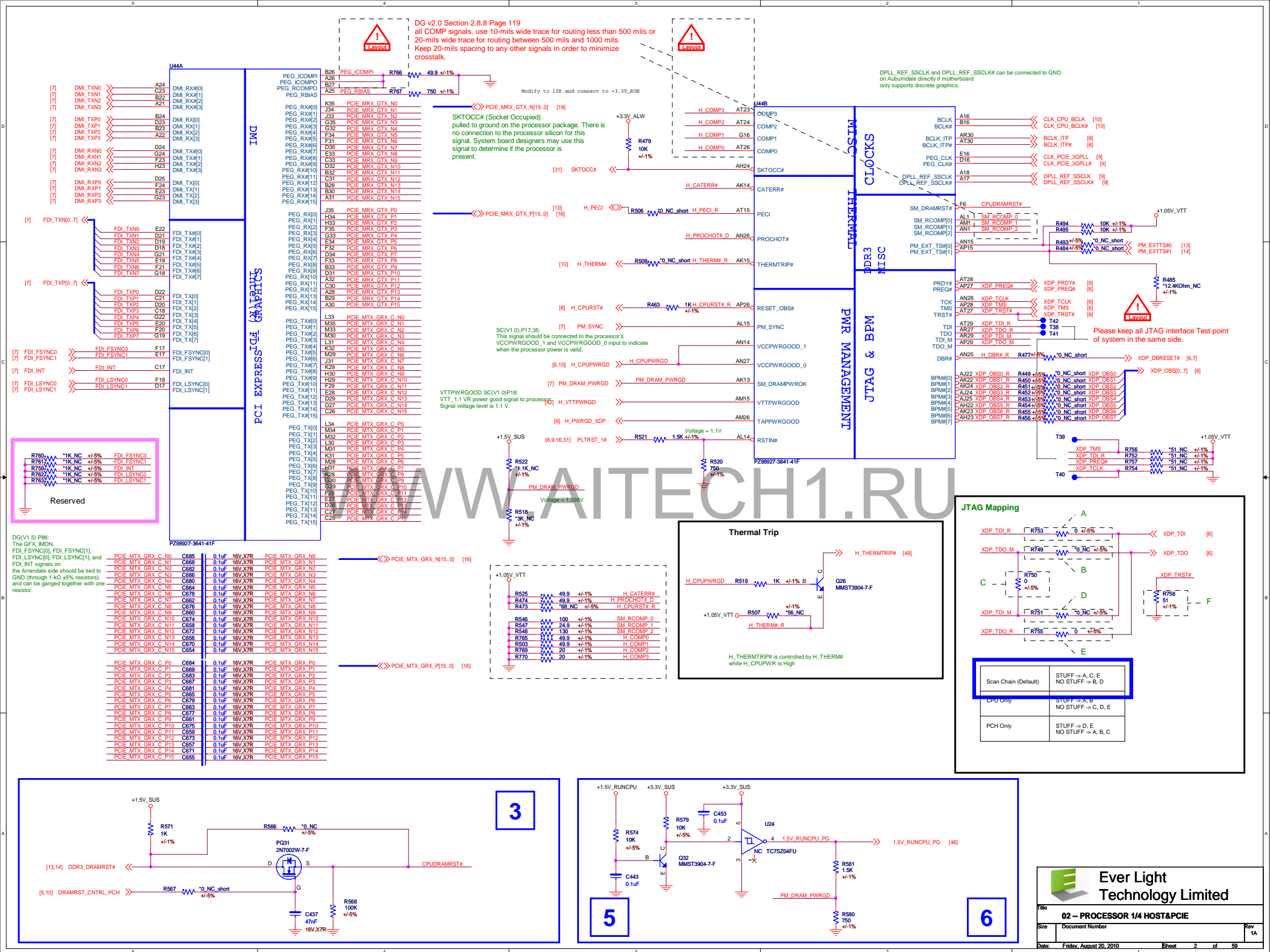


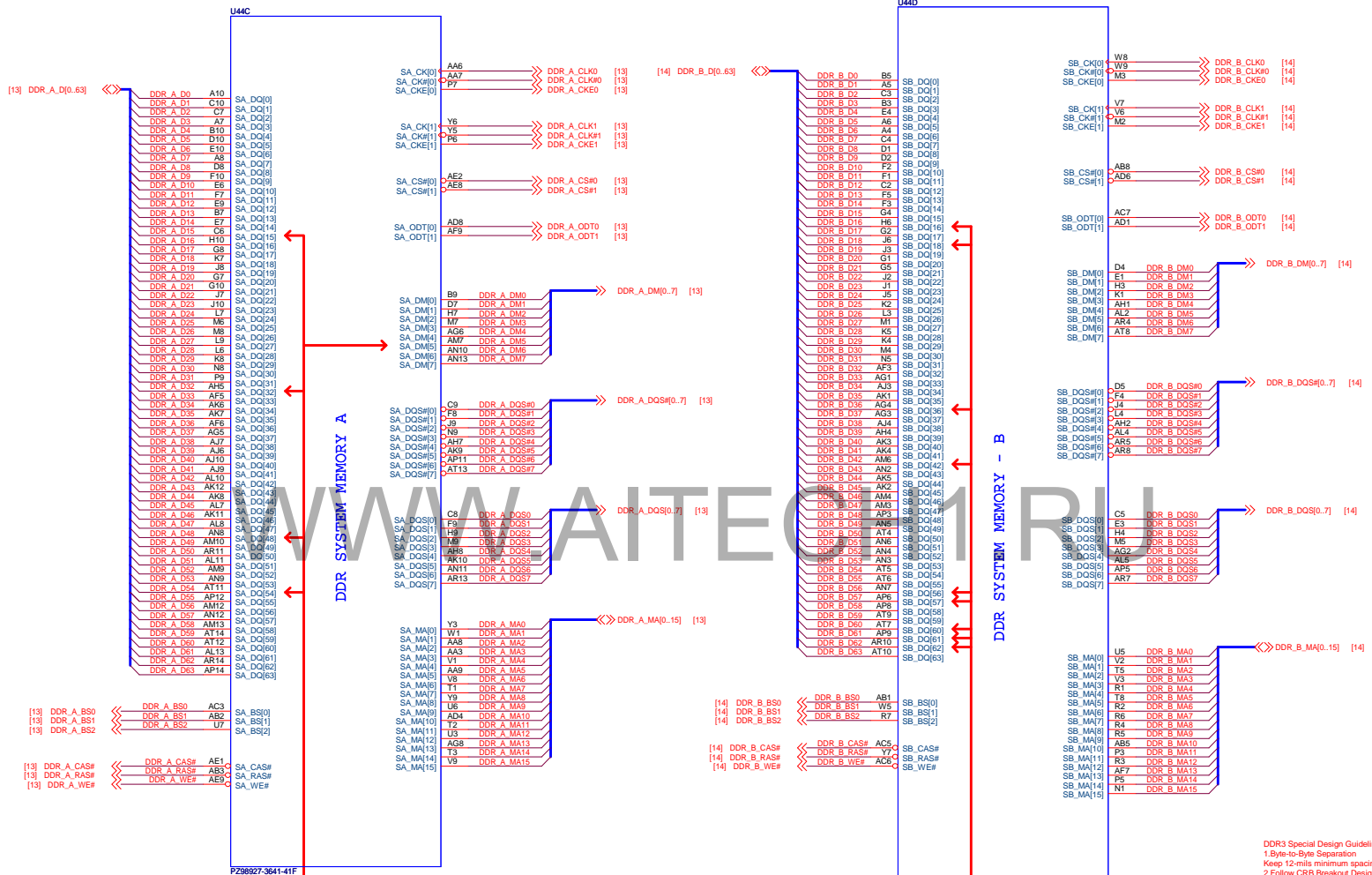
Nichols 14" Calpella DIS Block Diagram



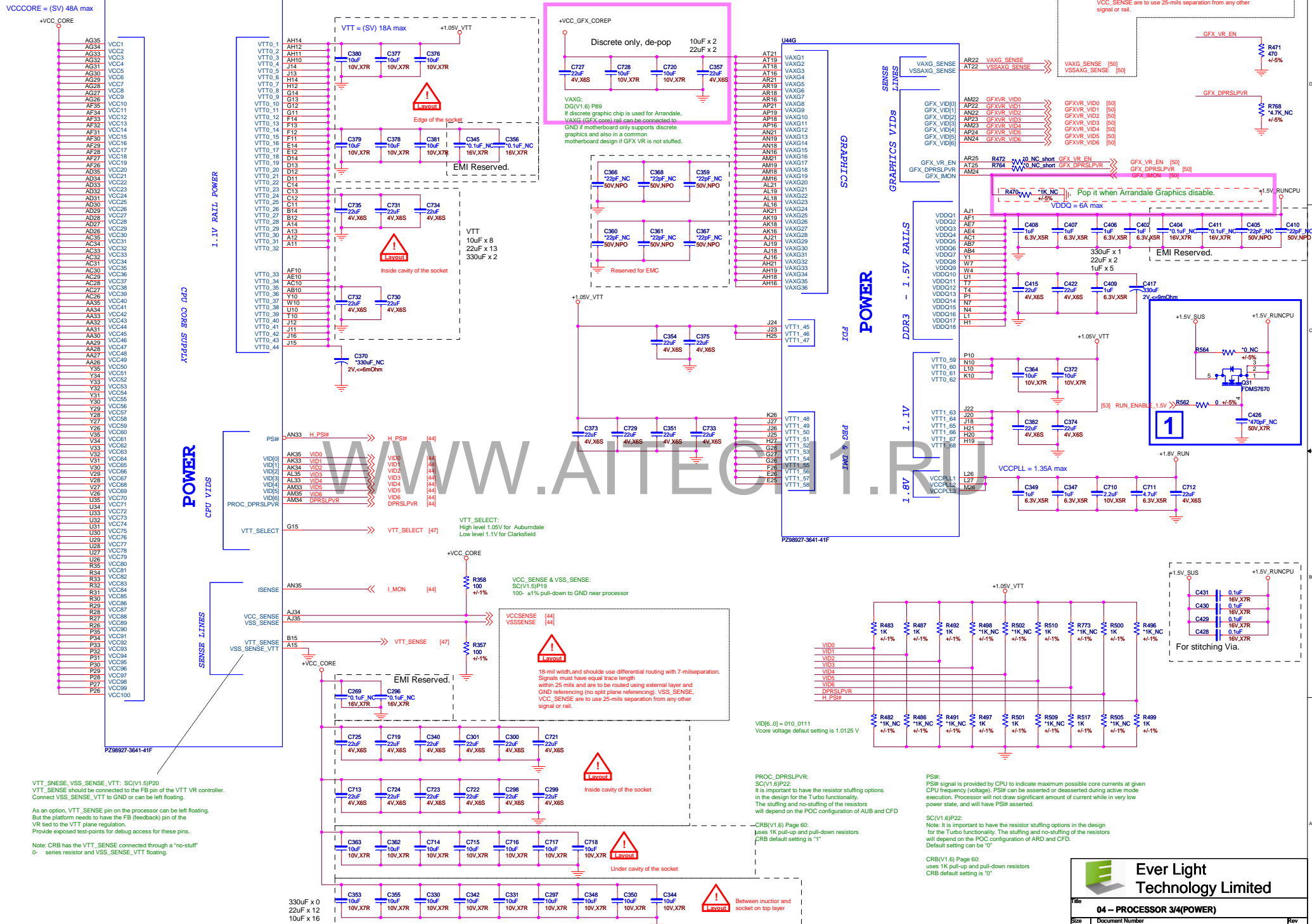
Ever Light Technology Limited



ARRANDALE PROCESSOR (DDR3)



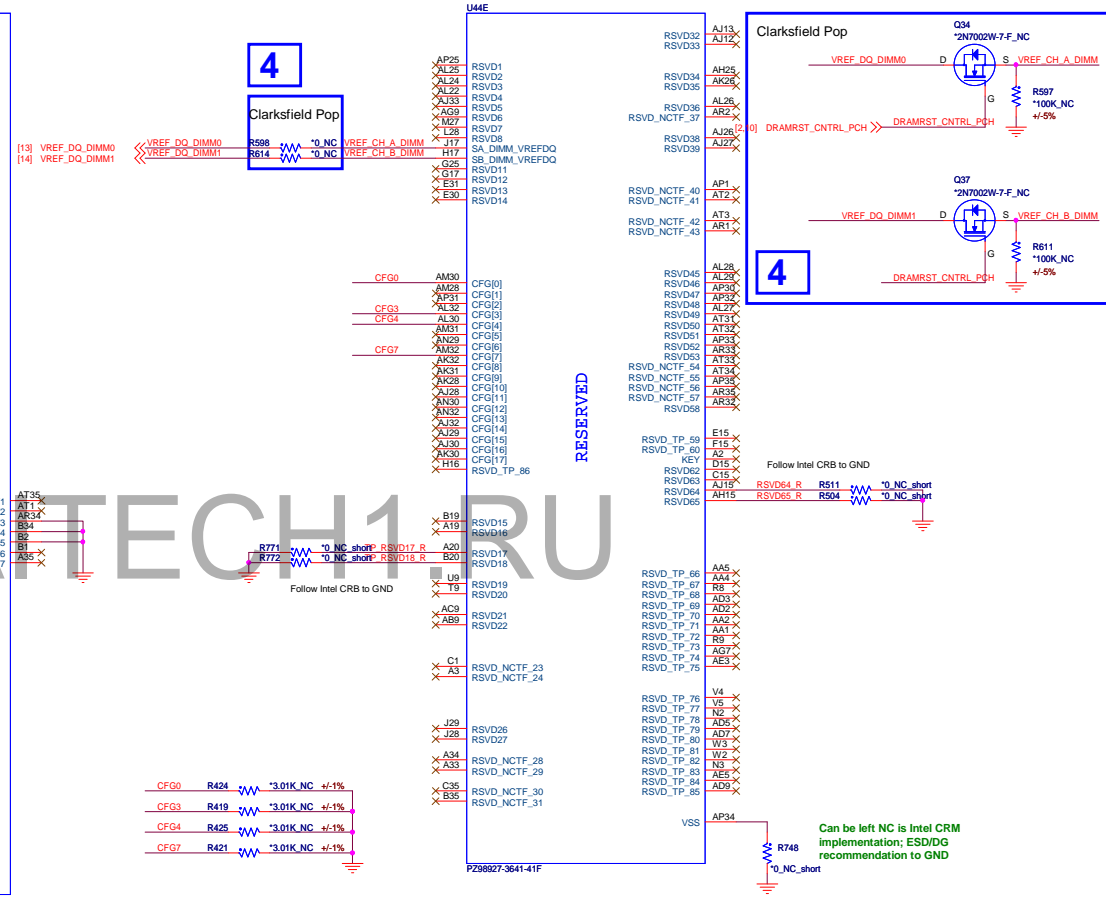
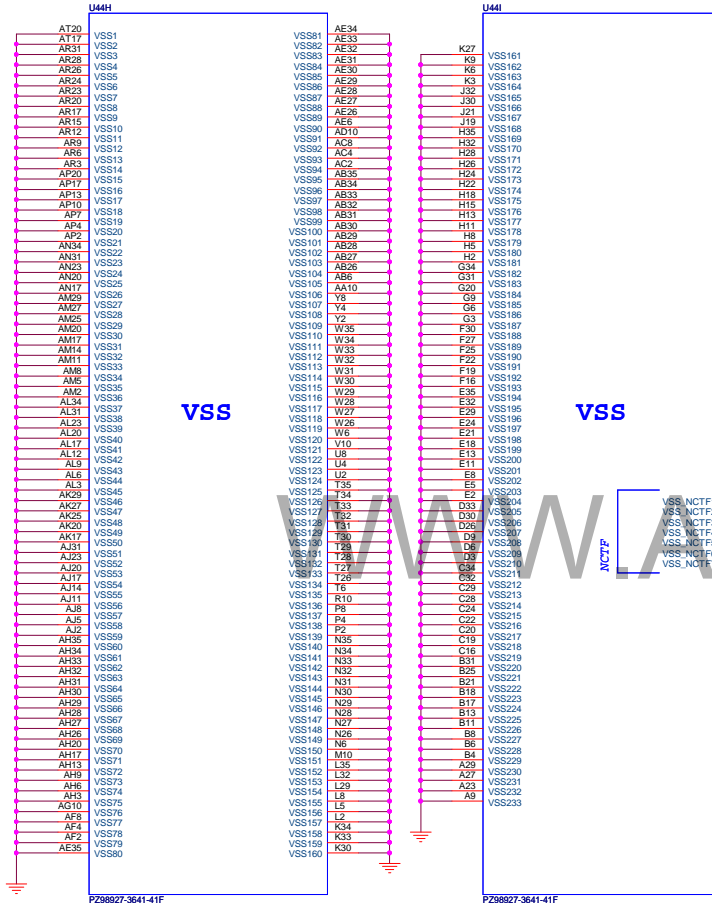
ARRANDALE PROCESSOR (GRAPHICS POWER)



M3

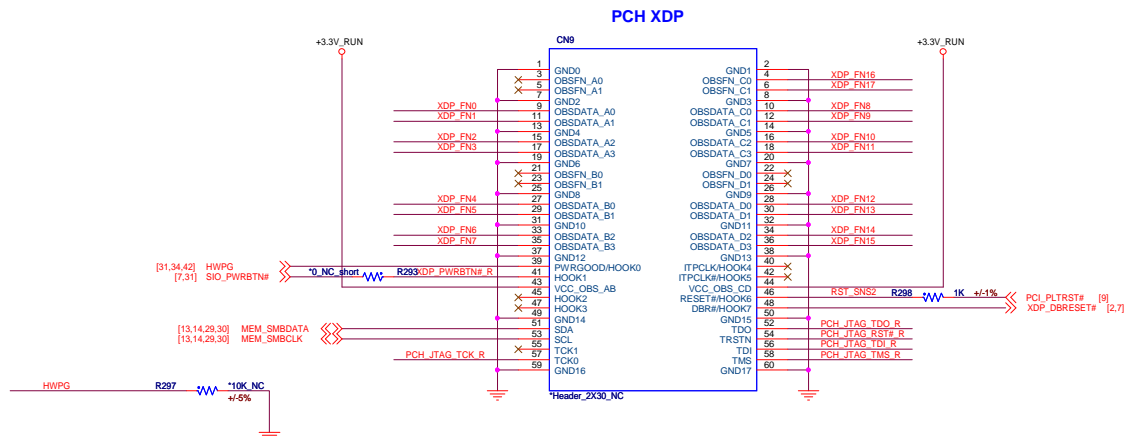
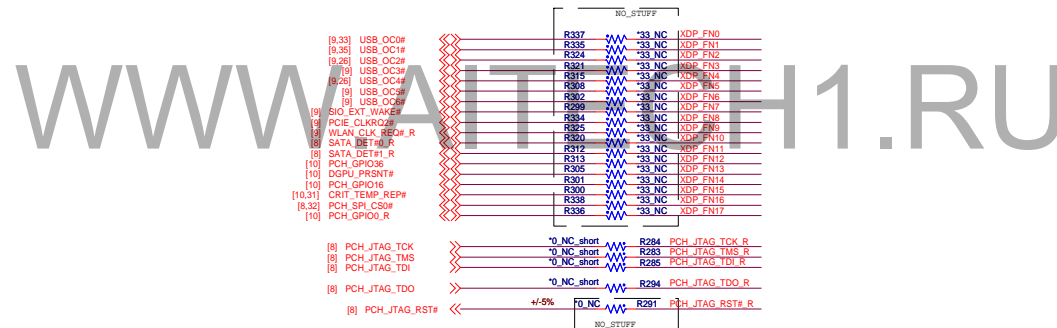
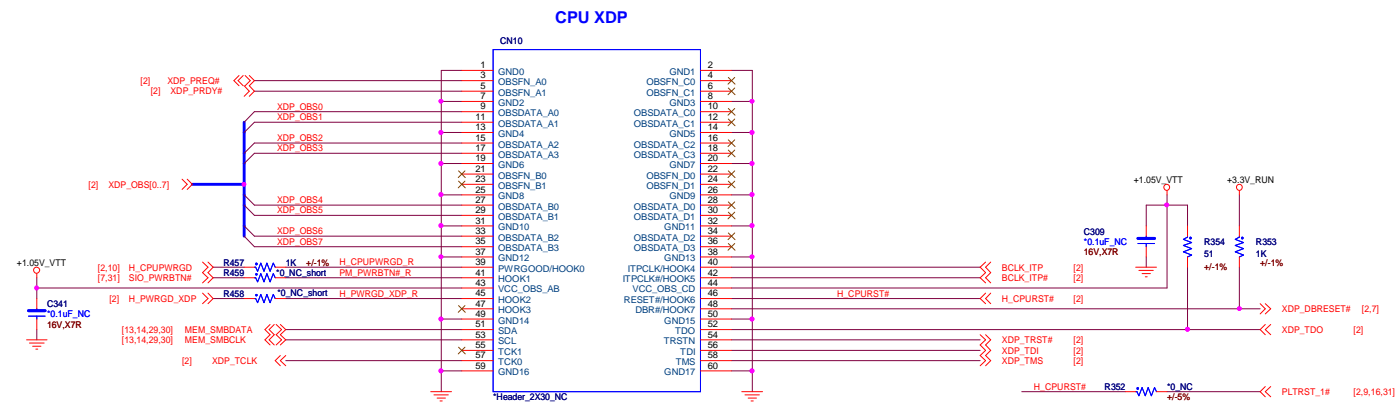
ARRANDALE PROCESSOR (GND)

ARRANDALE PROCESSOR(RESERVED, CFG)

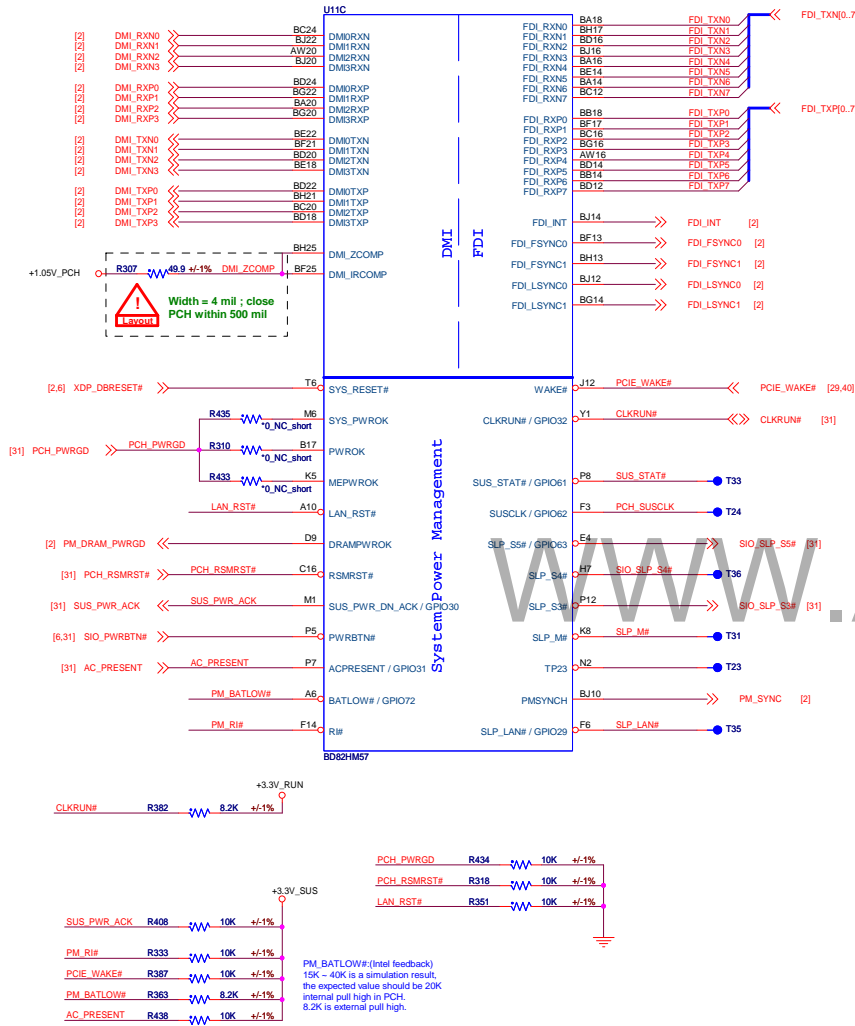


The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

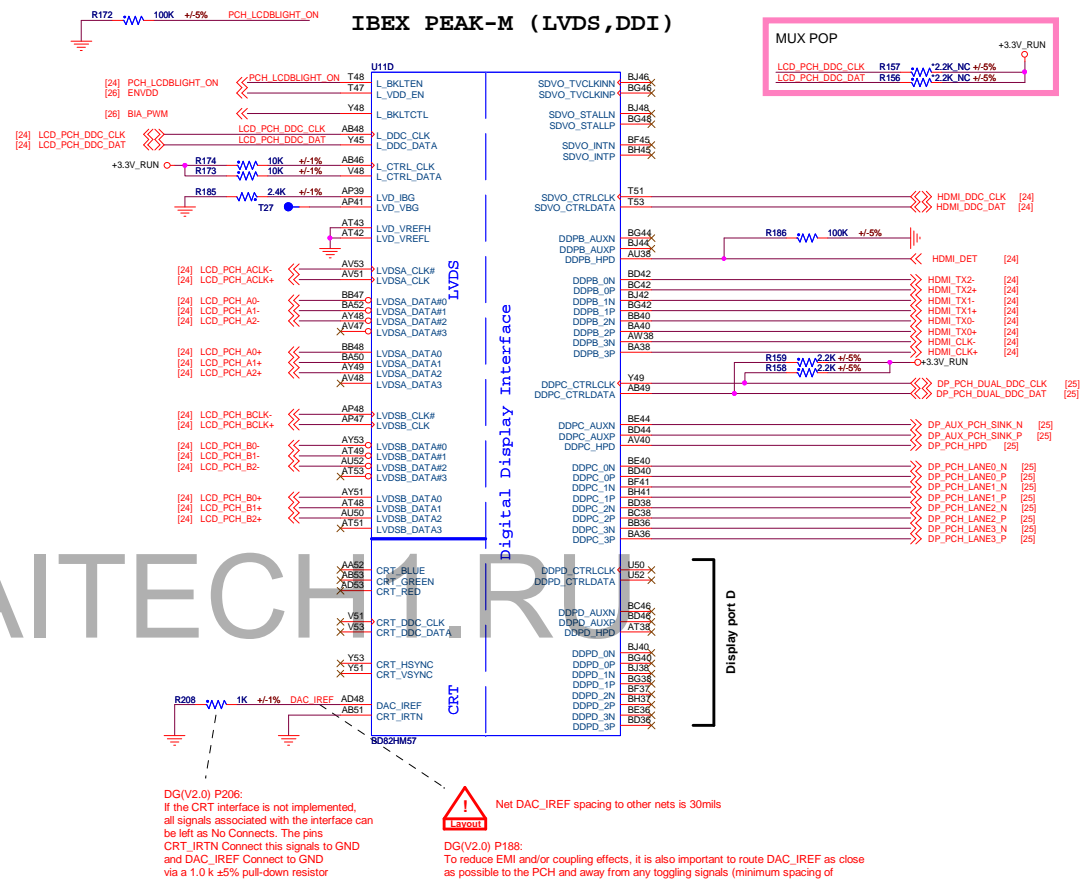
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port (Default Value)	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG (Default Value)	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation (Default Value)	Lane Numbers Reversed



1116



IBEX PEAK-M (LVDS,DDI)



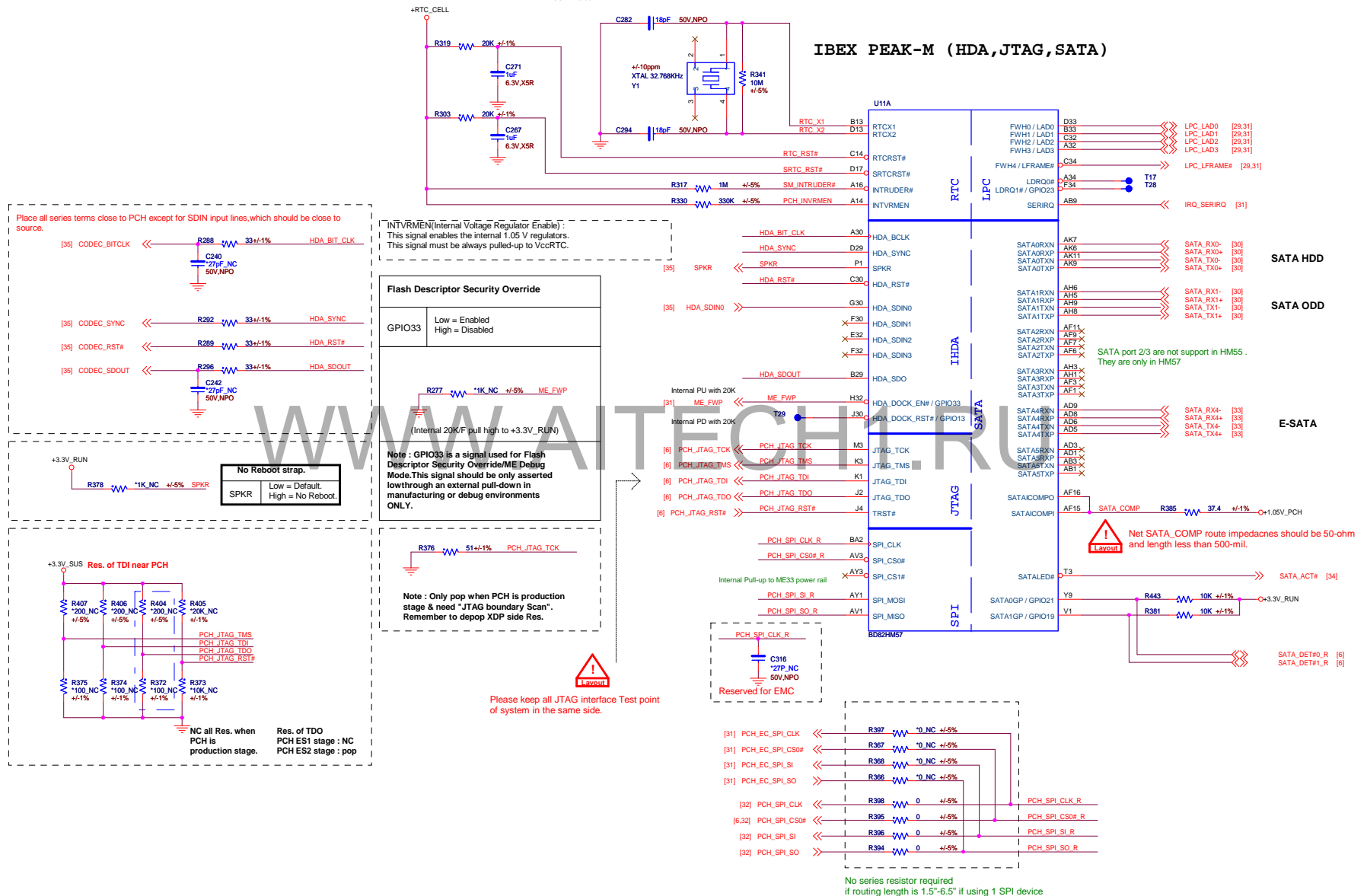
DG(V2.0) P206:
If the CRT interface is not implemented, all signals associated with the interface can be left as No Connects. The pins CRT_IJRTN Connect this signals to GND and DAC_IREF Connect to GND via a 1.0 k $\pm 5\%$ pull-down resistor

 Net DAC_IREF spacing to other nets is 30mils

DG(V2.0) P188:
To reduce EMI and/or coupling effects, it is also important to route DAC_IREF as close as possible to the PCH and away from any toggling signals (minimum spacing of 30 mils or 0.762 mm). No specific trace width or trace impedance is required for this signal. Routing DAC_IREF close to any toggling signals distorts the display. Distortion may vary from blinking/burning dots, rippling lines, wavy lines, etc

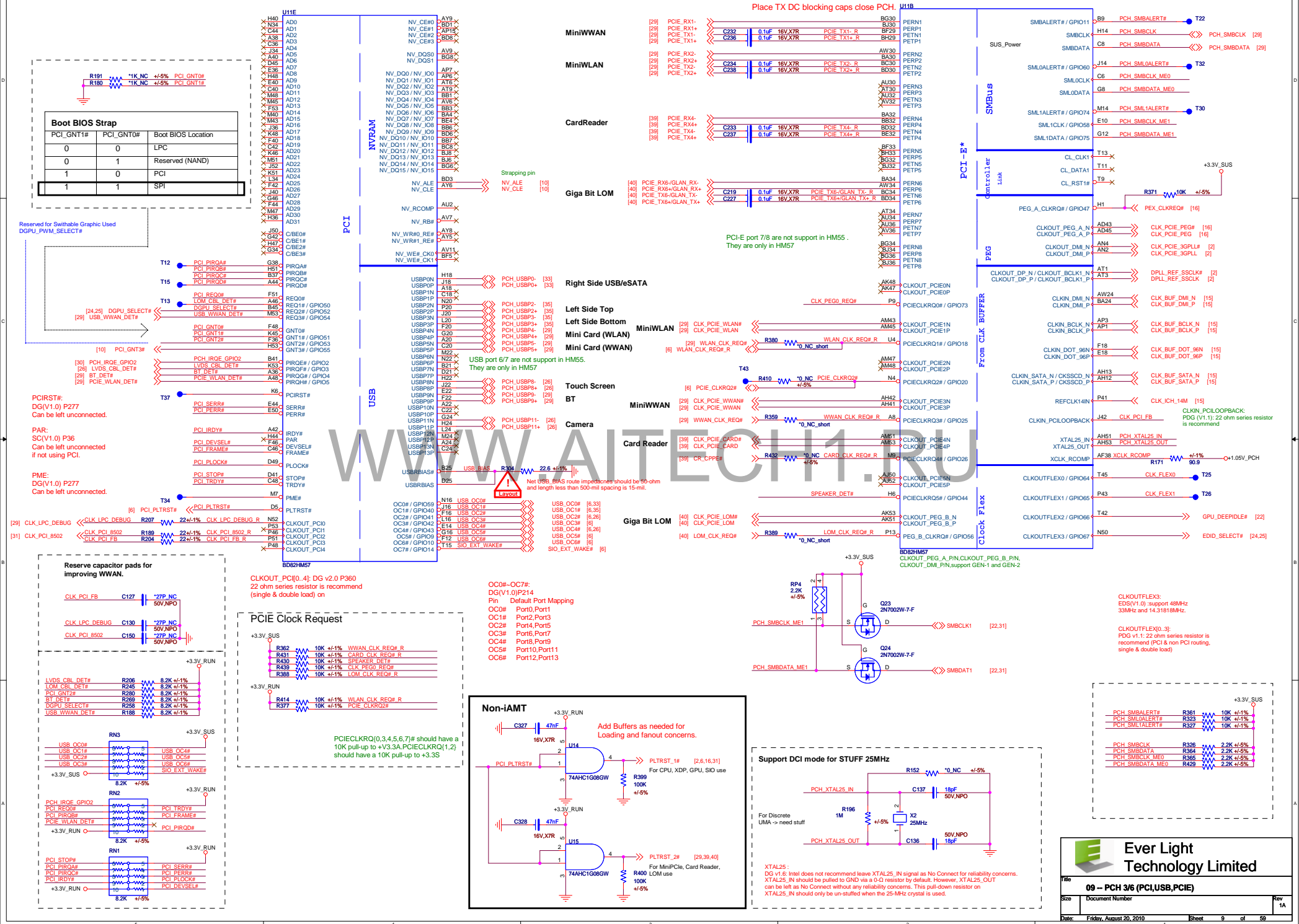
Scott_0727:Change Y1 PN to 710104400-310-G,footprint to x4s69x14h14

IBEX PEAK-M (HDA,JTAG,SATA)

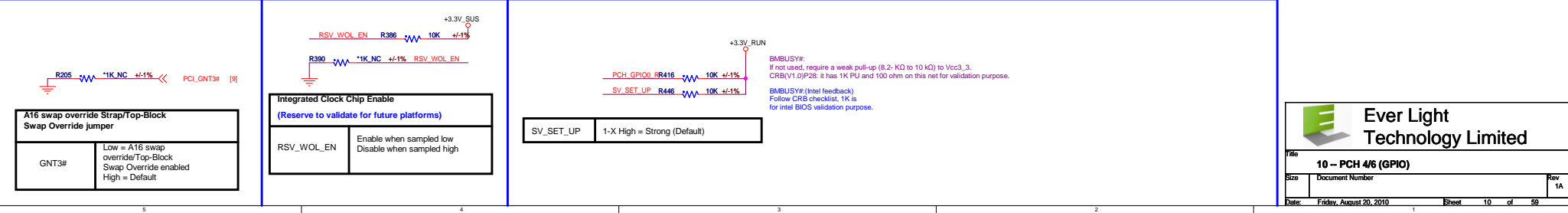


IBEX PEAK-M (PCI,USB,NVRAM)

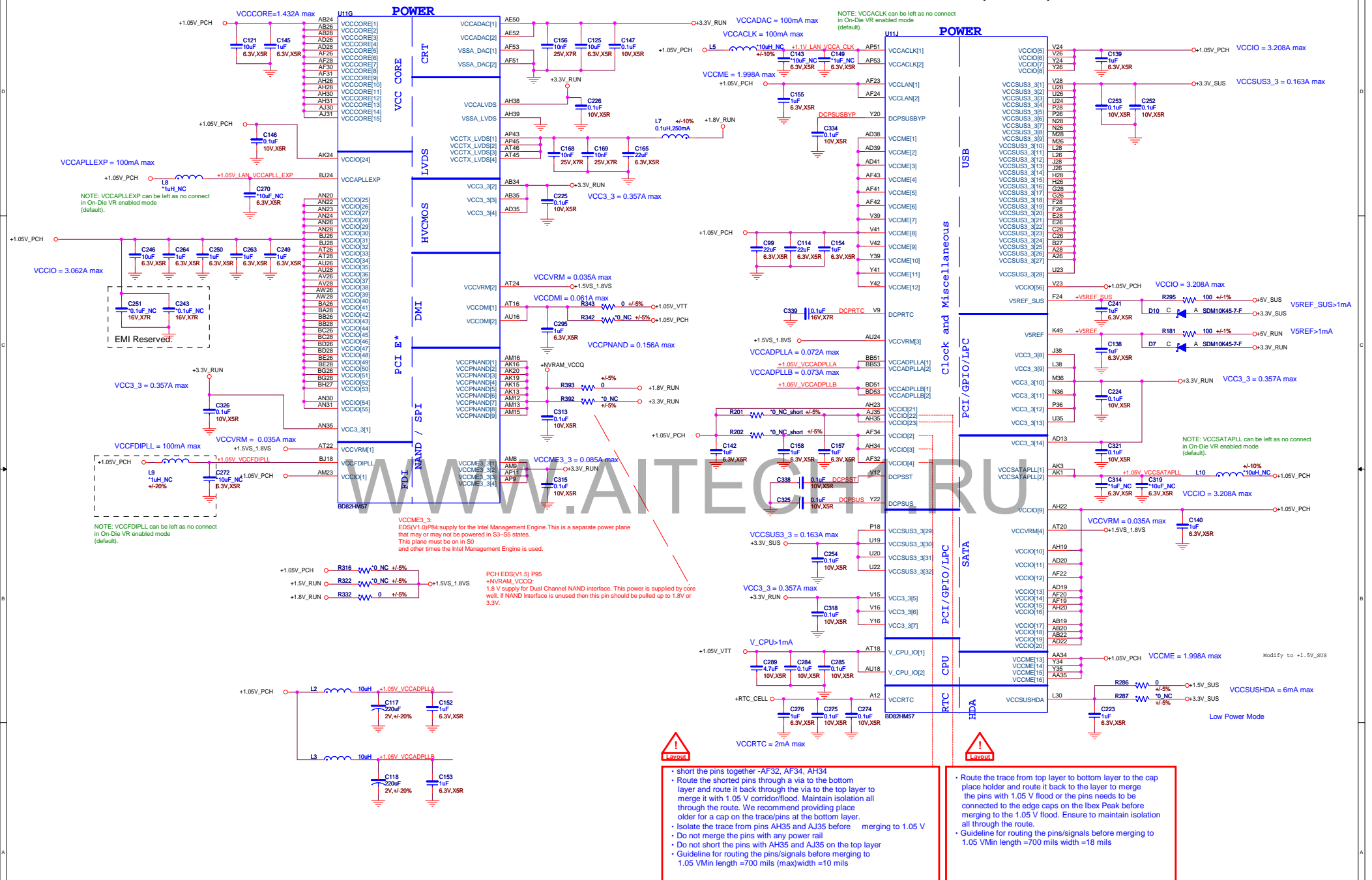
IBEX PEAK-M (PCI-E,SMBUS,CLK)



WWW.AI1TECH1.RU



IBEX PEAK-M (POWER)

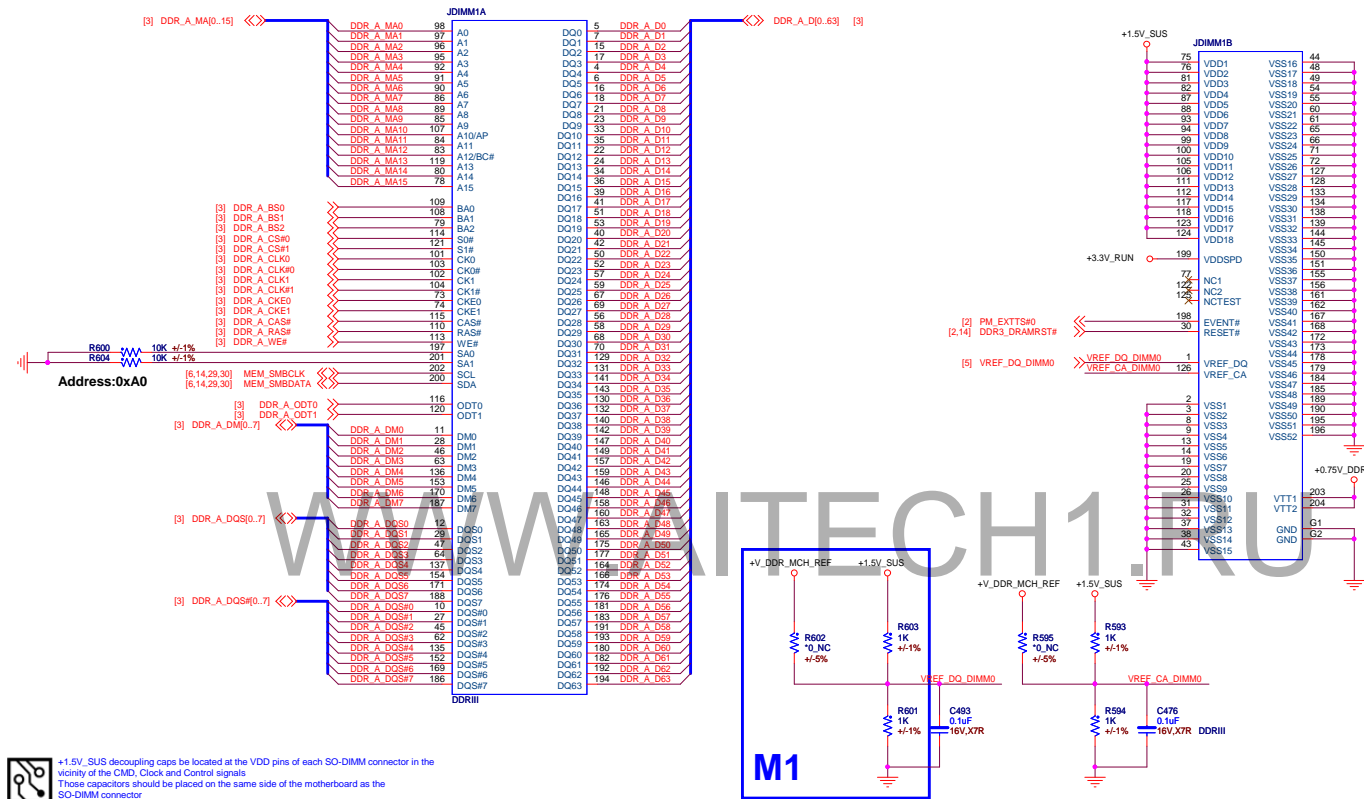


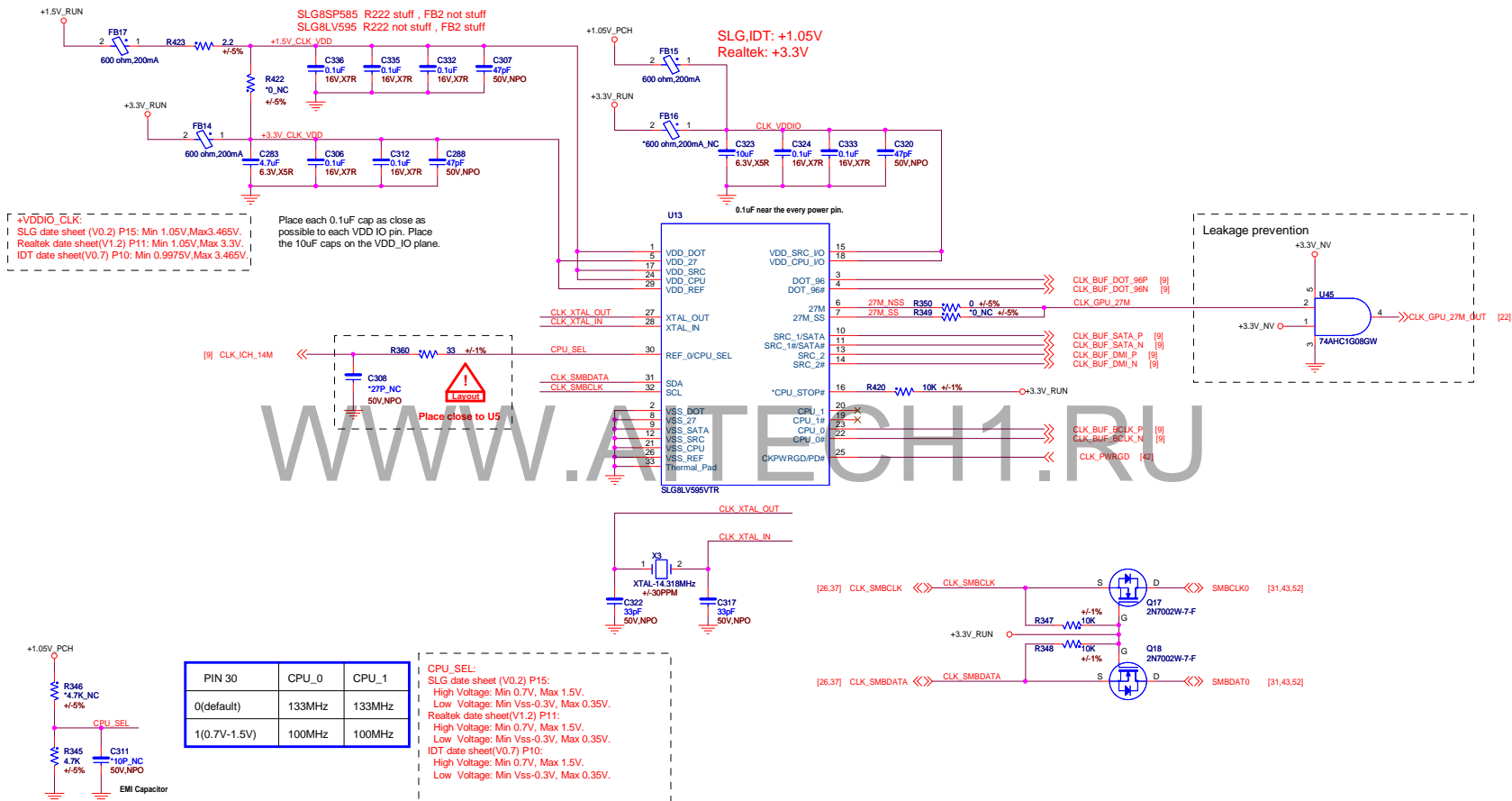
Ibex Peak DisplayPort interface may violate the Non ISI Jitter Measurements and Total Jitter Measurements tests due to the power delivery noise on specific VccIO pins.
This fix would also applicable to HDMI 1080P 60Hz Deep color mode.
Please see Intel Doc No.430877 Intel® I5 Series Chipset (Ibex Peak) DisplayPort* Jitter Technical Advisory



Title		
11 -- PCH 5/6 (POWER)		
Size	Document Number	Rev 1A
Date:	Friday, August 20, 2010	Sheet 11 of 59

DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils





Frame Buffer Interface

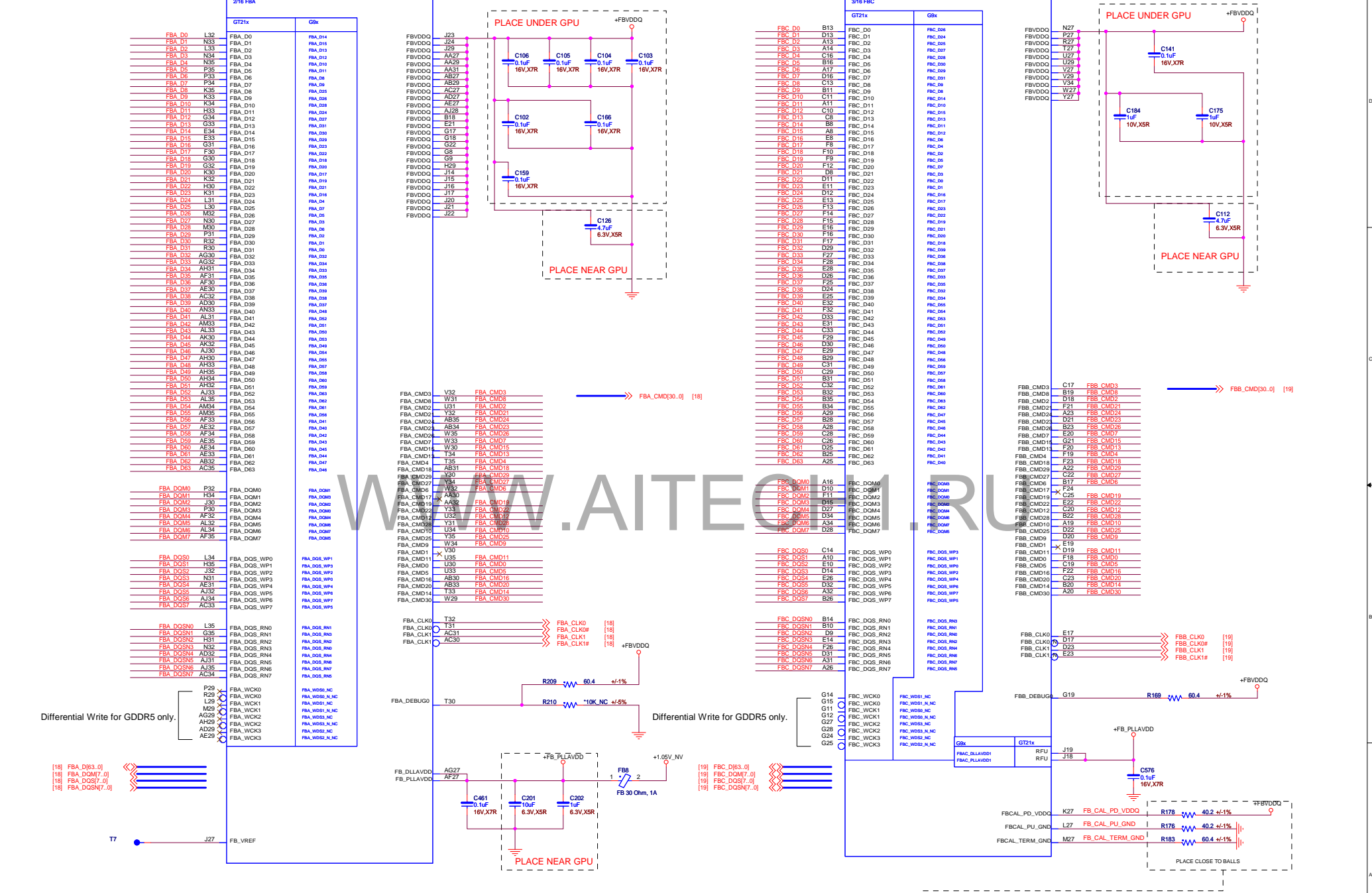



Table 3. Frame Buffer Calibration Resistor Values

Memory Type	FBVDDQ	FBAL_PU_GND	FBAL_PD_VDDQ	FBAL_TERM_GND
DDR3	1.5 V	40.2 Ω	40.2 Ω	60.4 Ω



Ever Light Technology Limited

17 – N11P 210(DDR3)


Size Document Number Rev 1A

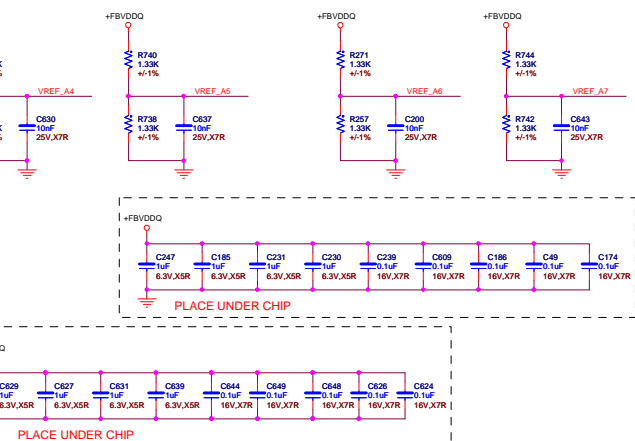
Date: Friday, August 20, 2010 Sheet 17 of 59

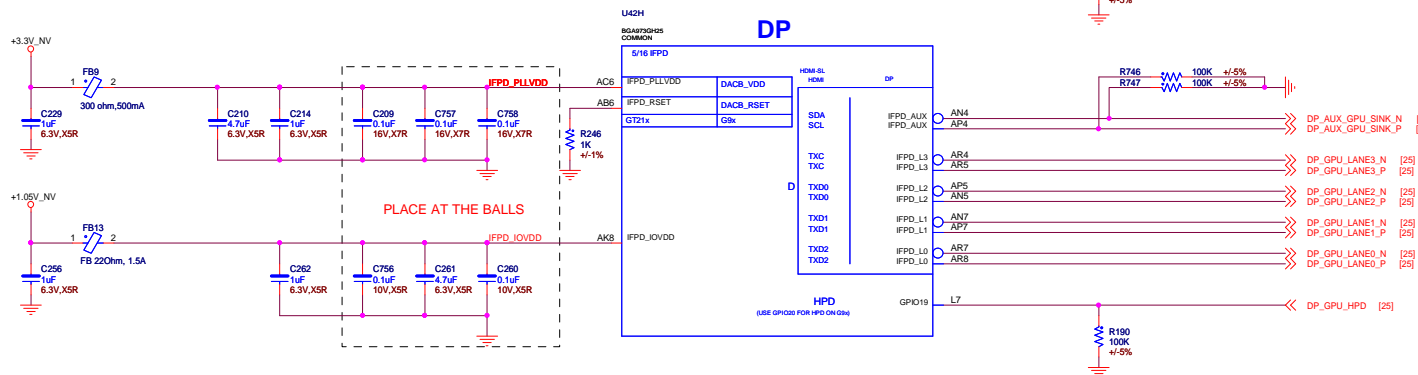
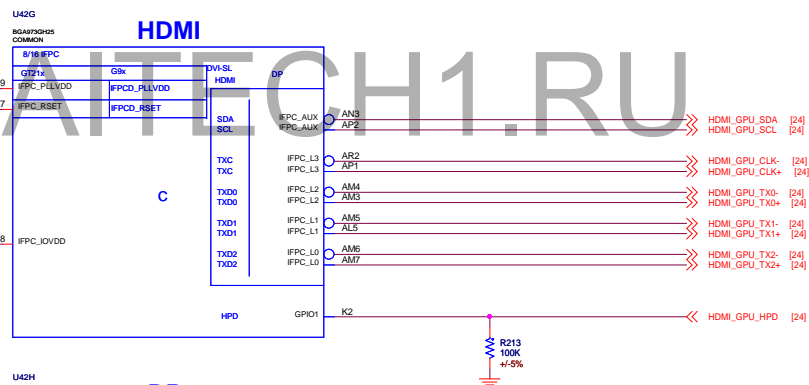
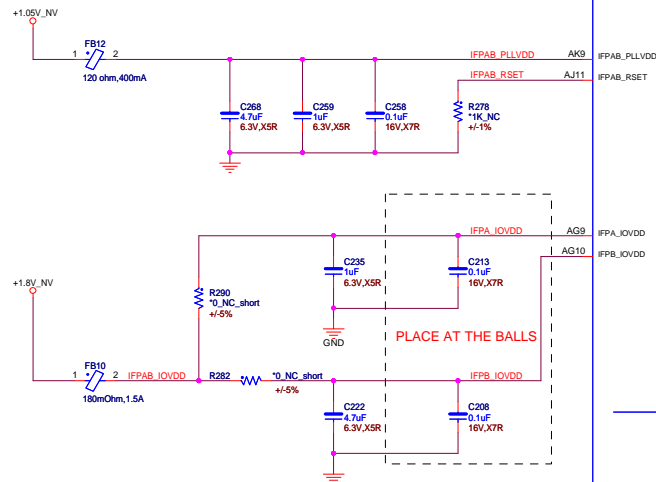
Memory Partition-A Upper Data Bits



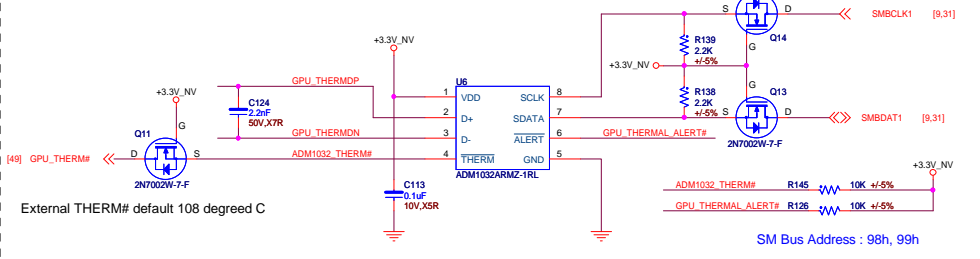
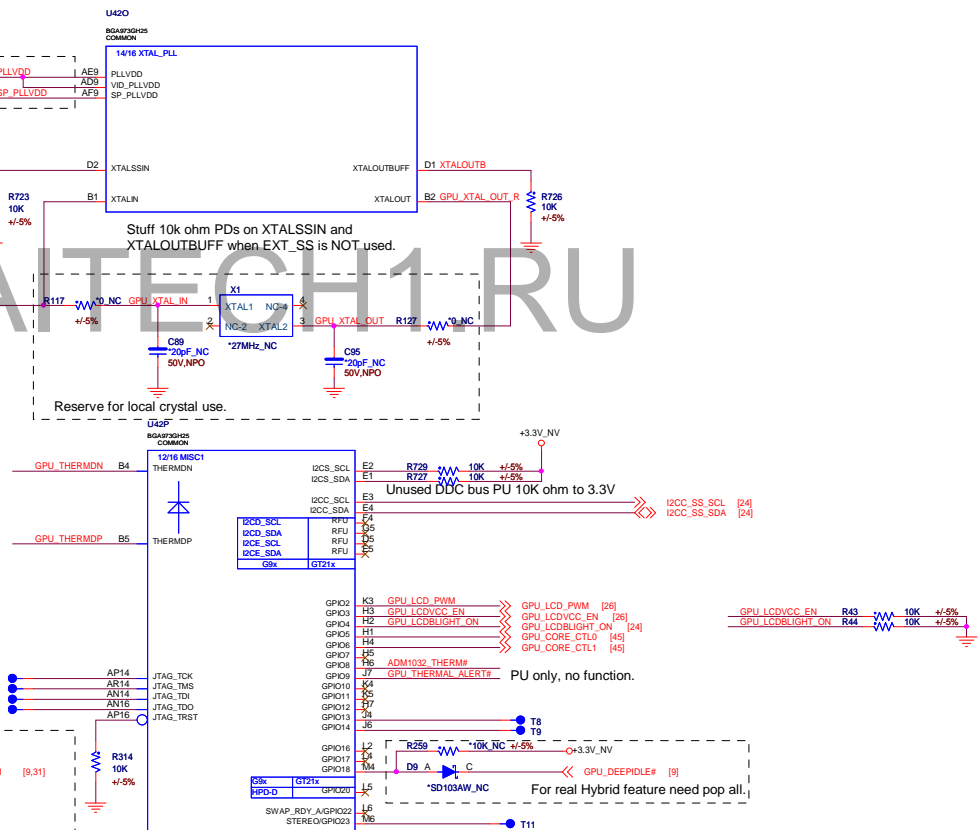
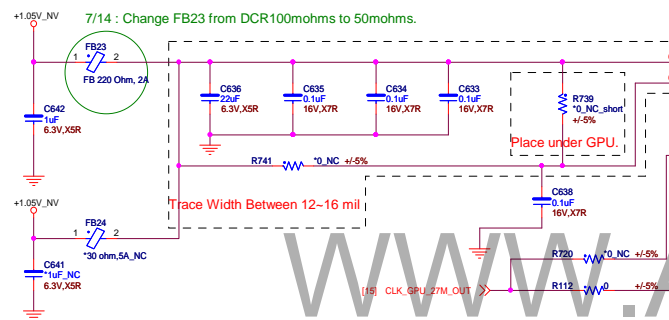
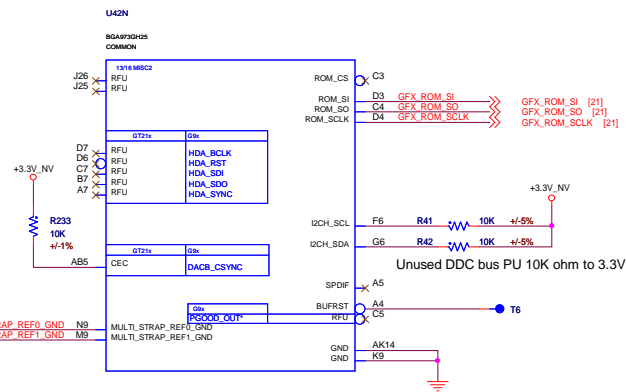
Table 5.4 Mode E Command Mapping

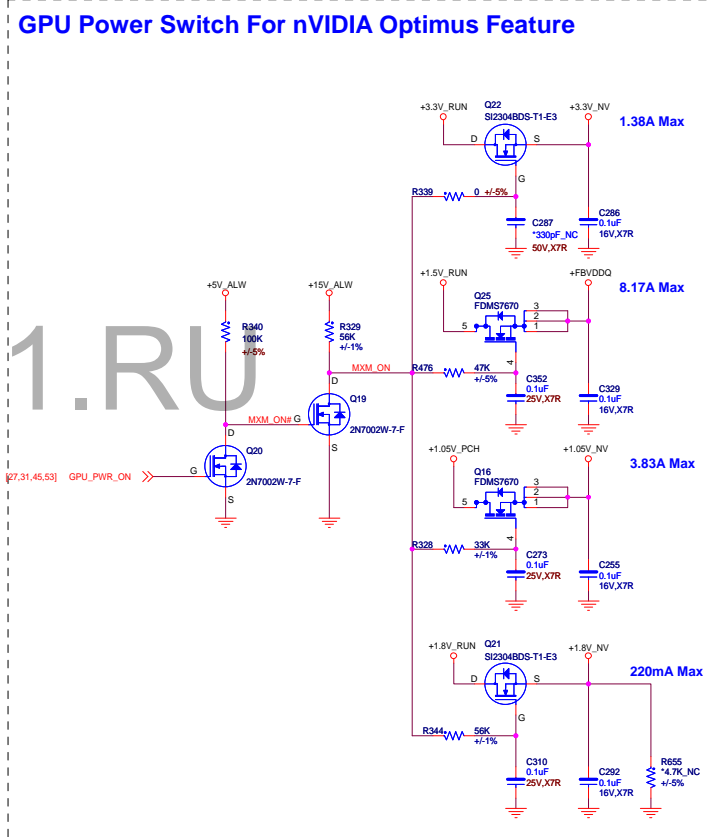
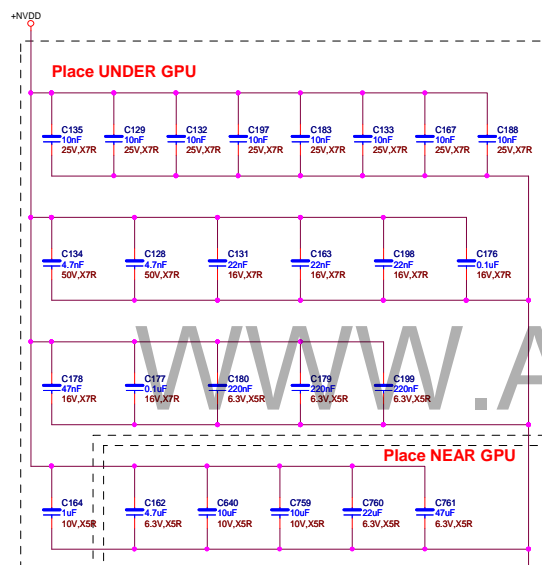
 <div> <div>Ever Light</div> <div>Technology Limited</div> </div>	
<div> <div>Title</div> <div>18 -- N11P 3/10(VRAM-A)</div> </div>	
<div> <div>Size</div> <div></div> </div>	<div> <div>Document Number</div> <div></div> </div>
<div> <div>Date: Friday, August 20, 2010</div> <div>Sheet 18 of 59</div> <div>Rev 1A</div> </div>	



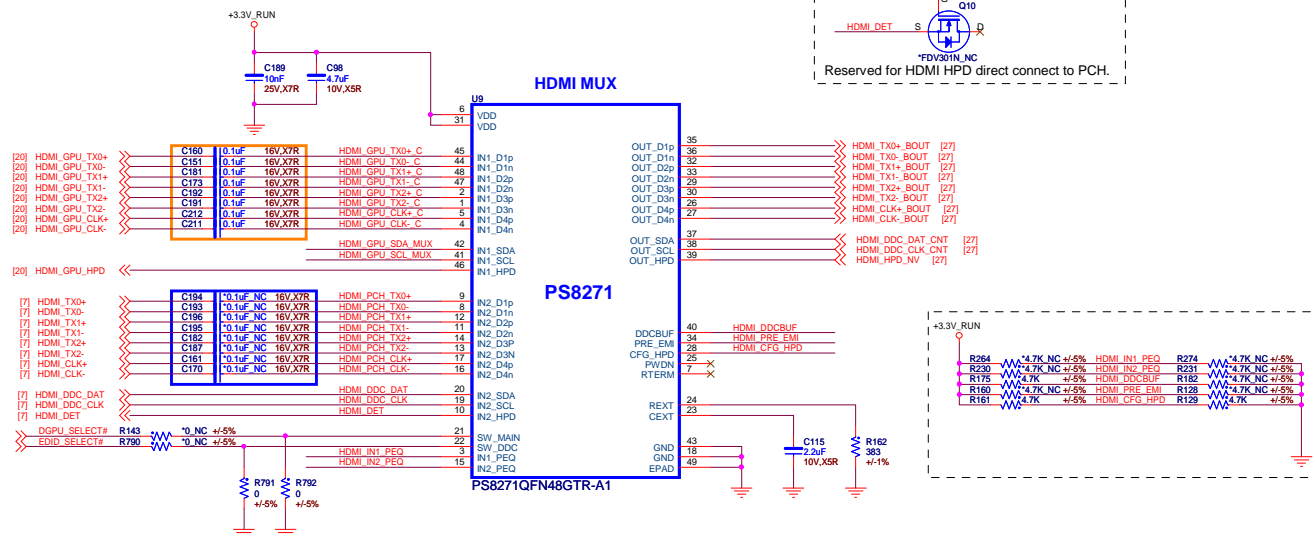
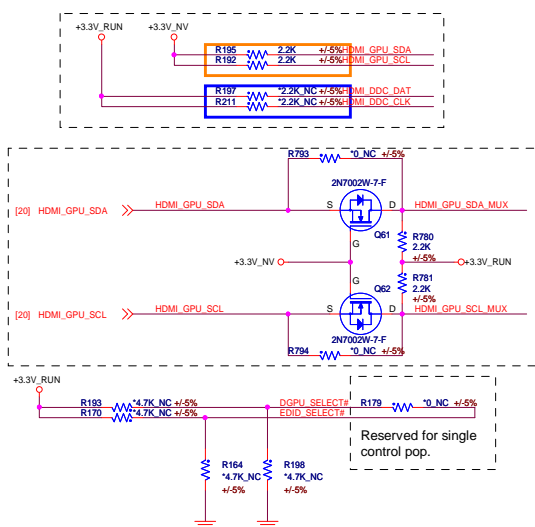
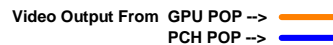


Mode	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND	Strapping Resistor for other STRAP pins
Binary Production Strapping	40.2 k Ω , 1% to GND	NC	10 k Ω , 5%
Multi-level Strapping	40.2 k Ω , 1% to GND	40.2 k Ω , 1% to GND	Refer to section 13.1

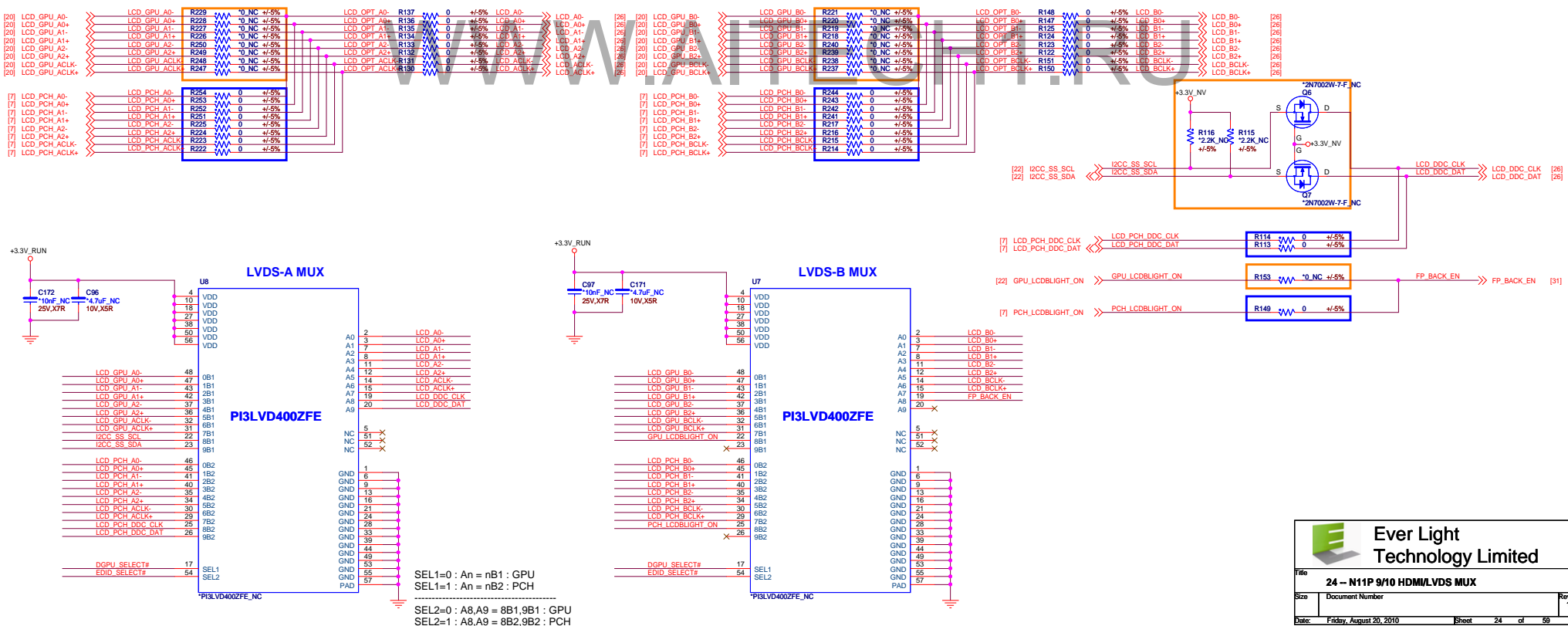




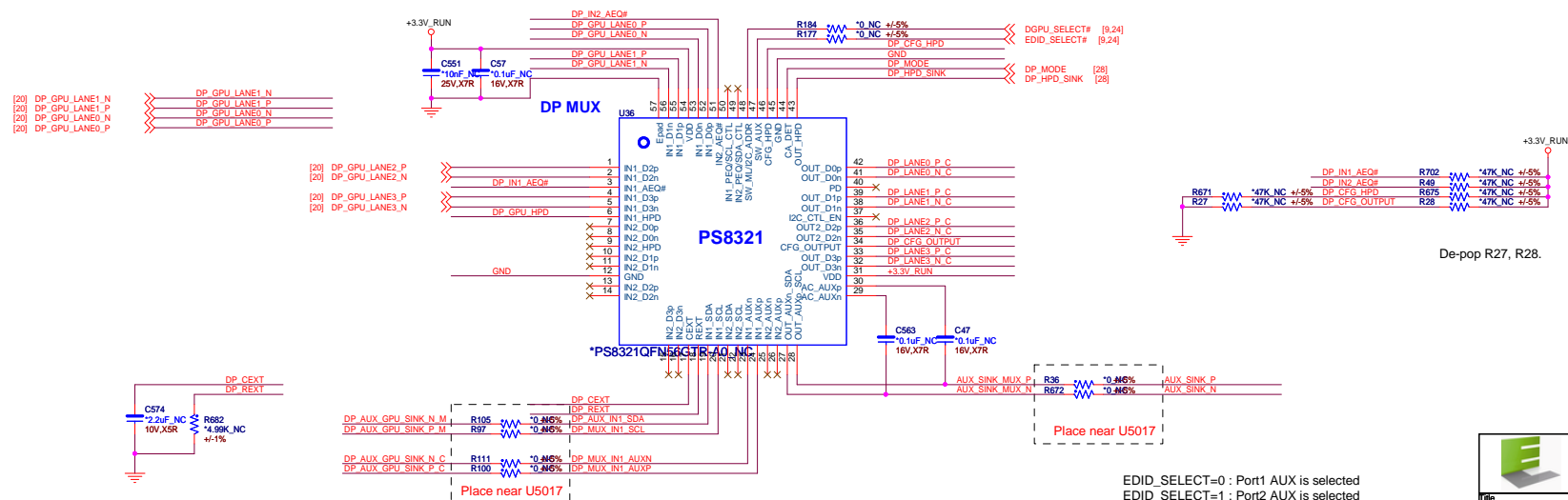
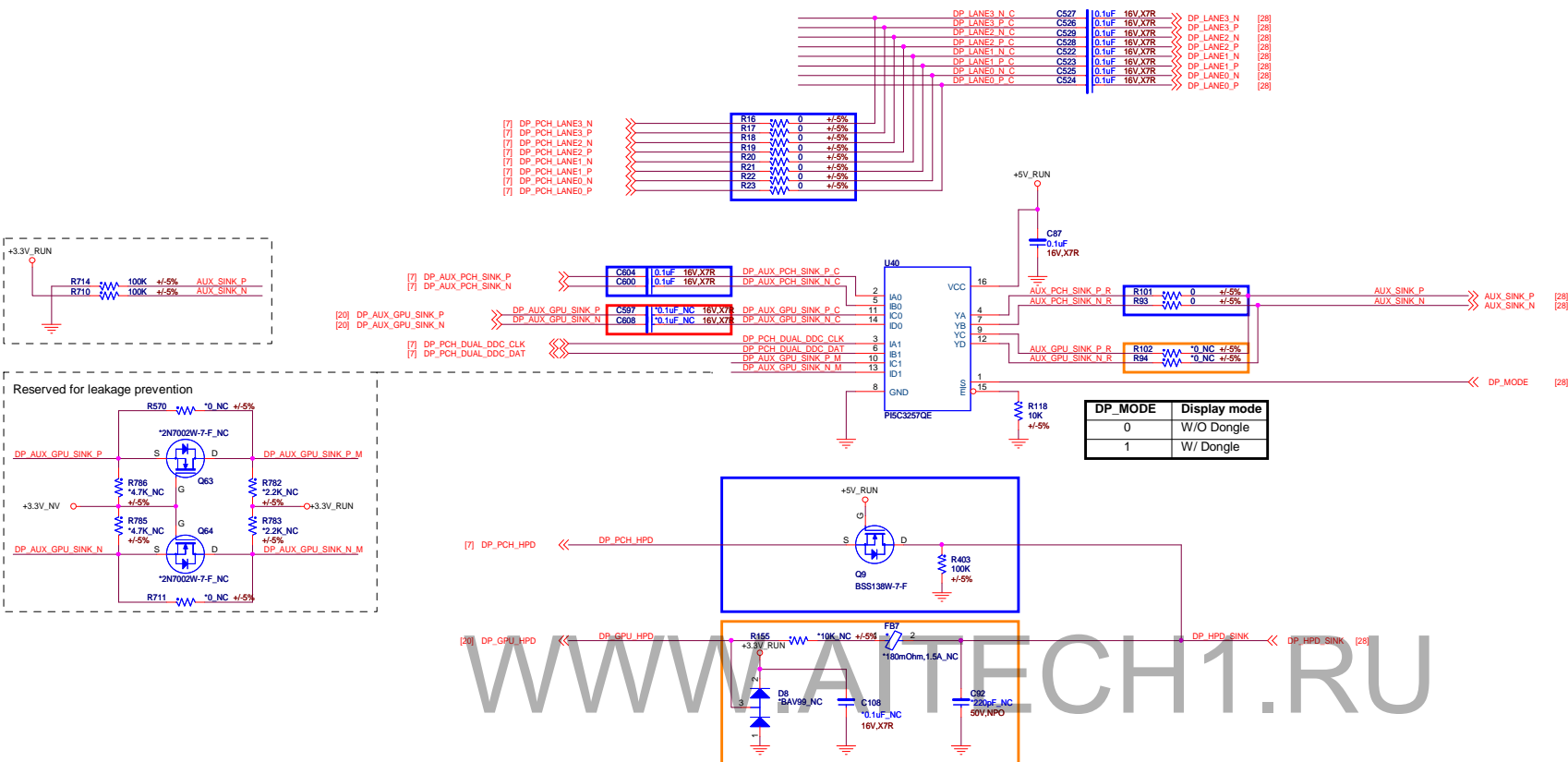
HDMI Display Option



LVDS Display Option

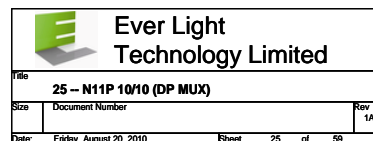


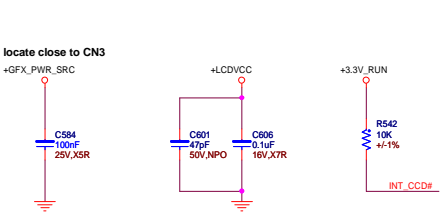
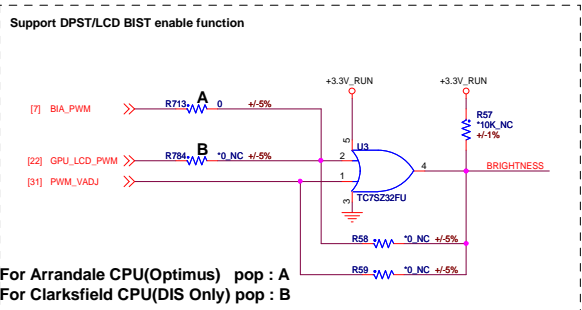
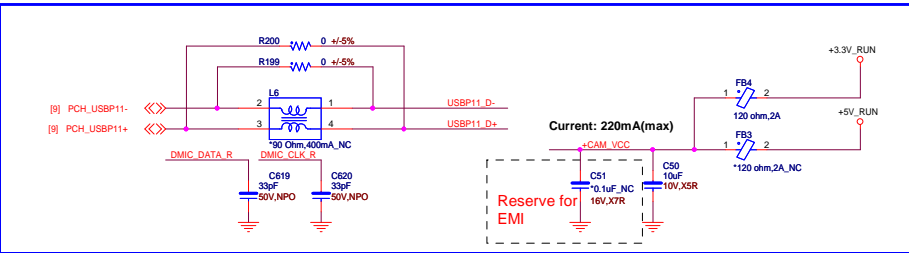
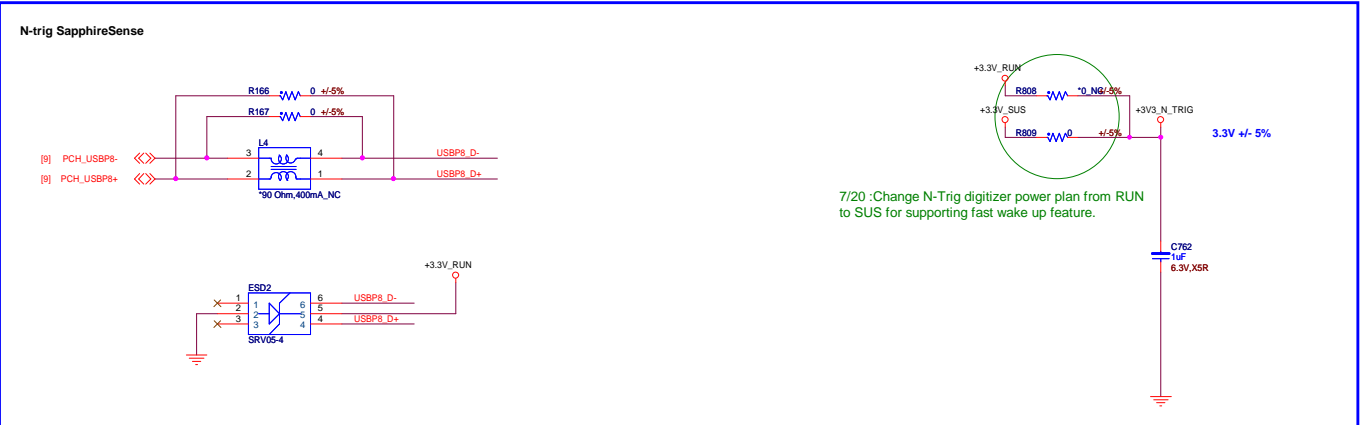
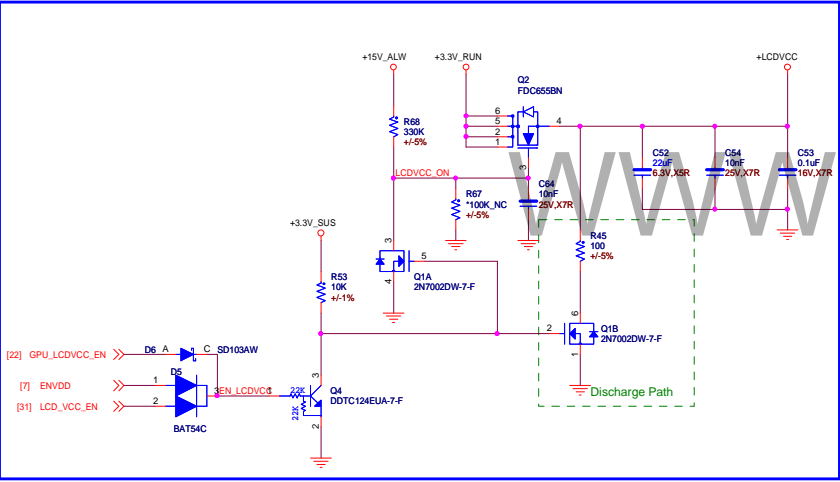
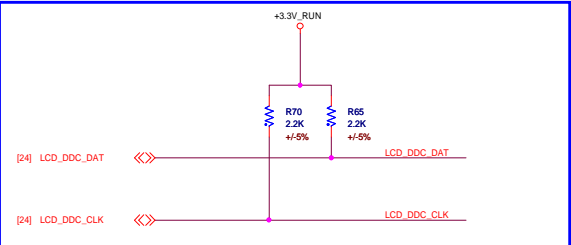
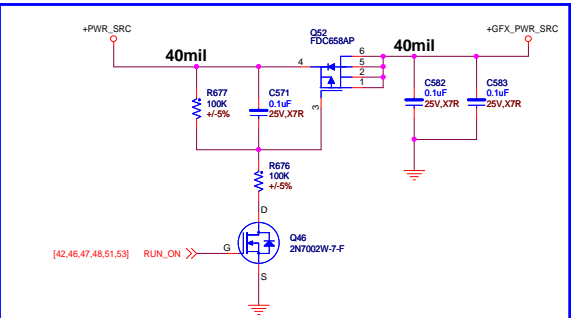
Video Output From GPU POP -->  DIS or UMA only
PCH POP -->



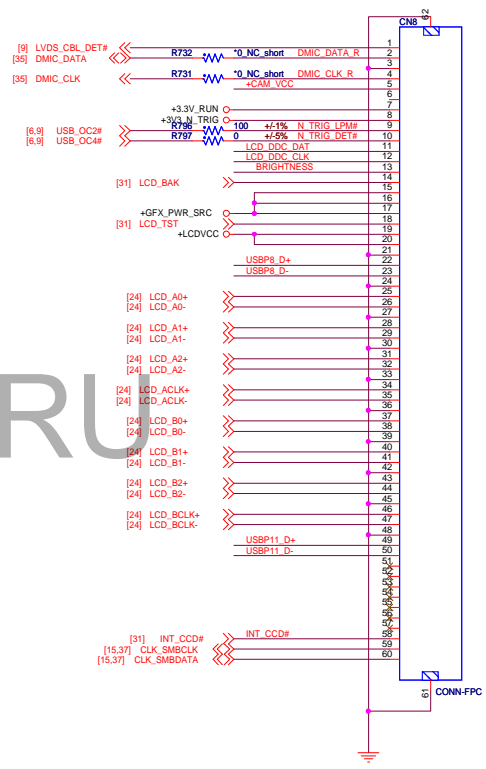
EDID_SELECT=0 : Port1 AUX is selected
EDID_SELECT=1 : Port2 AUX is selected

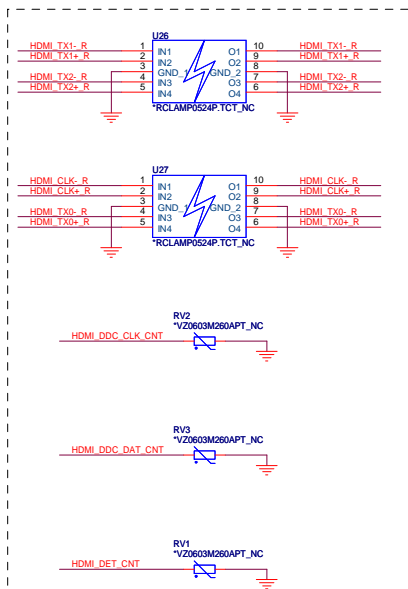
dGPU_SELECT#=0 : Port1 main lane and HPD is selected.
dGPU_SELECT#=1 : Port2 main lane and HPD is selected.



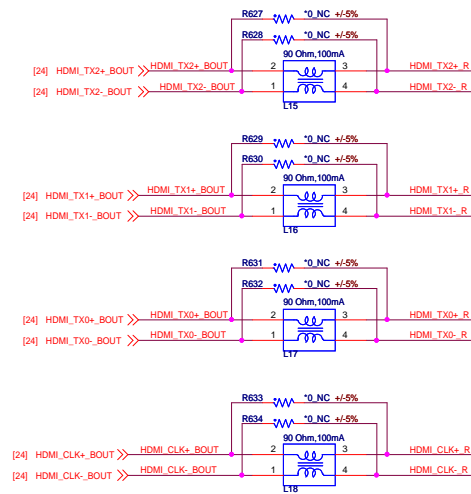


Address : A9H --Contrast
AAH --Backlight

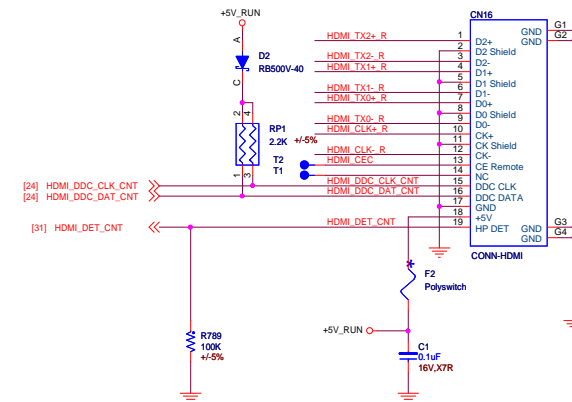




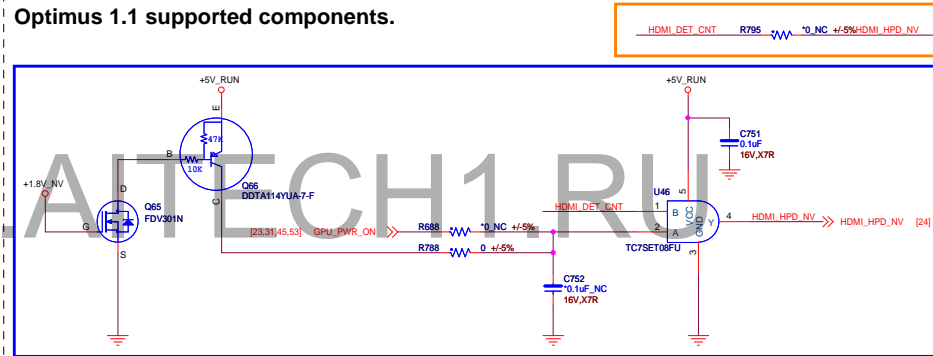
Reserve for EMI and close to HDMI CONN

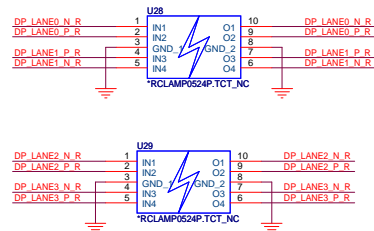
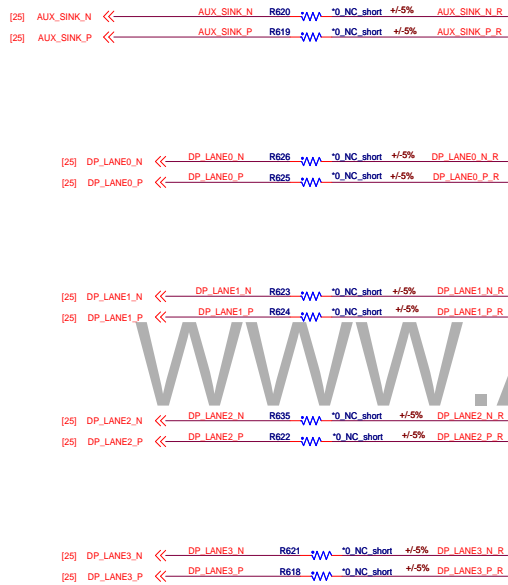


HDMI

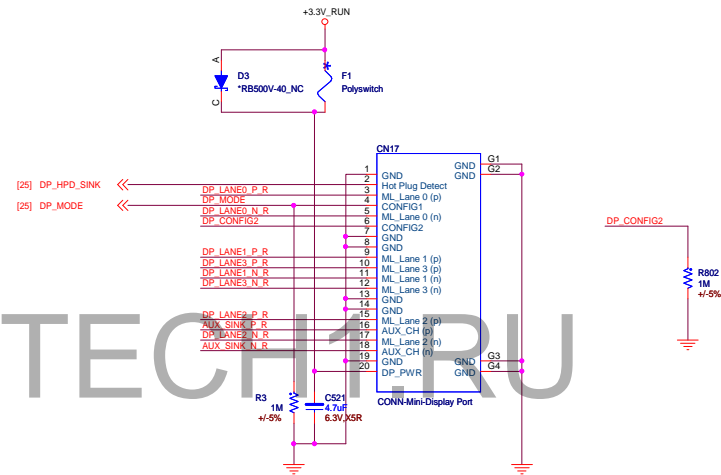


Optimus 1.1 supported components.

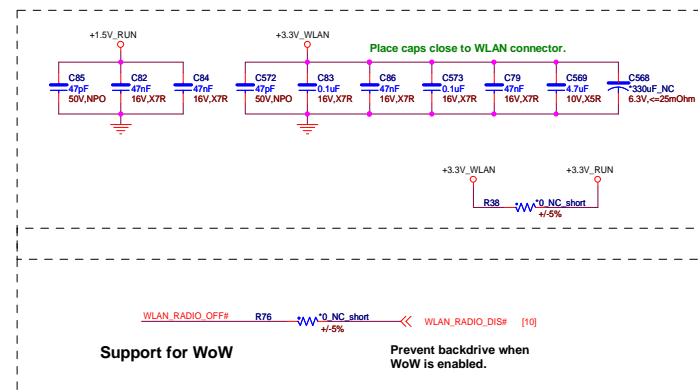
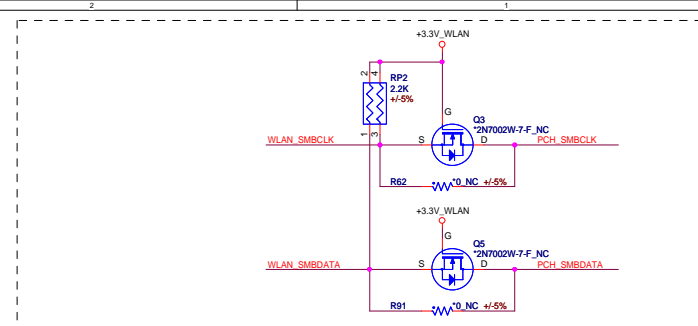
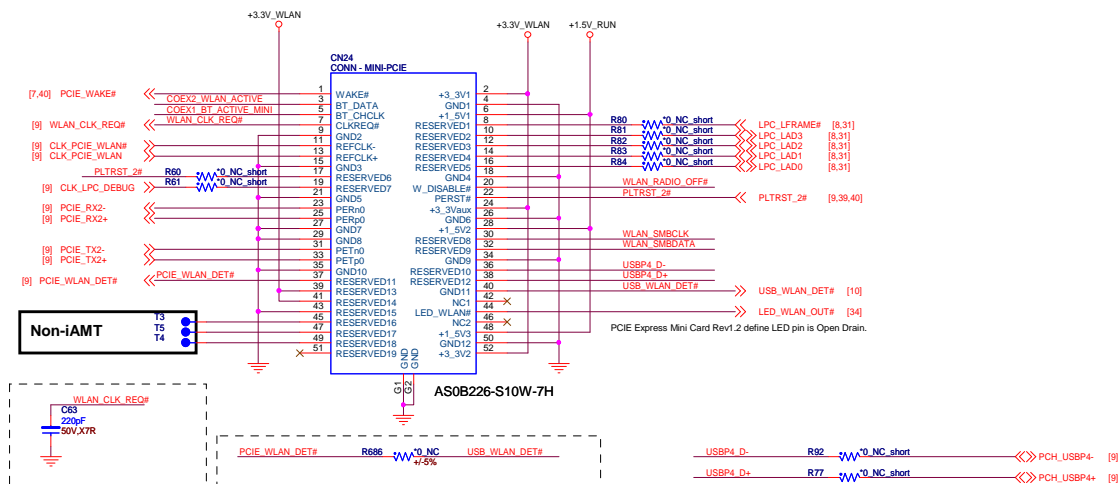




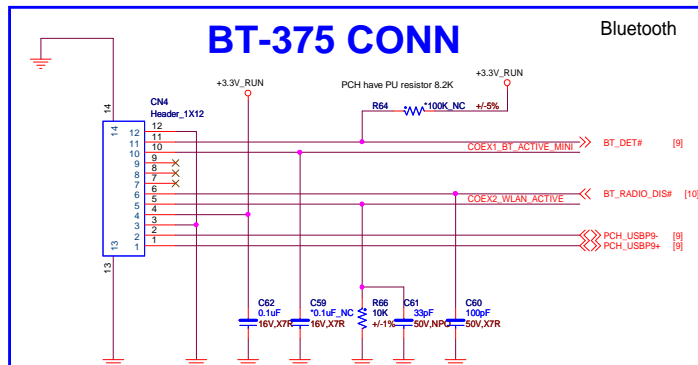
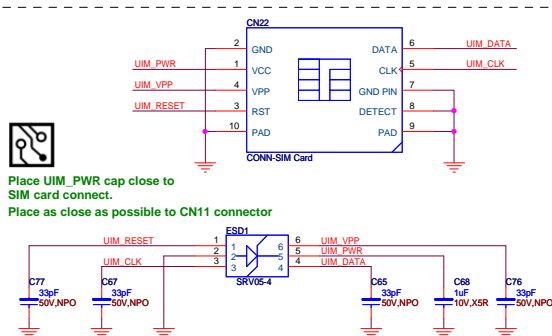
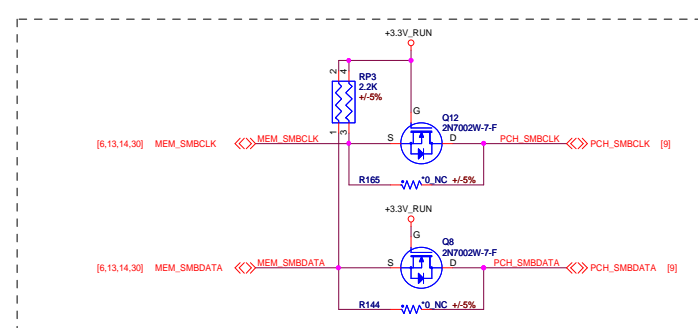
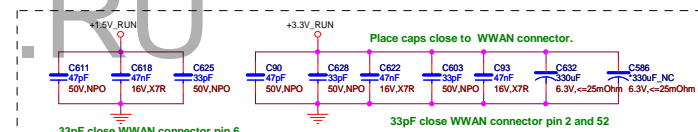
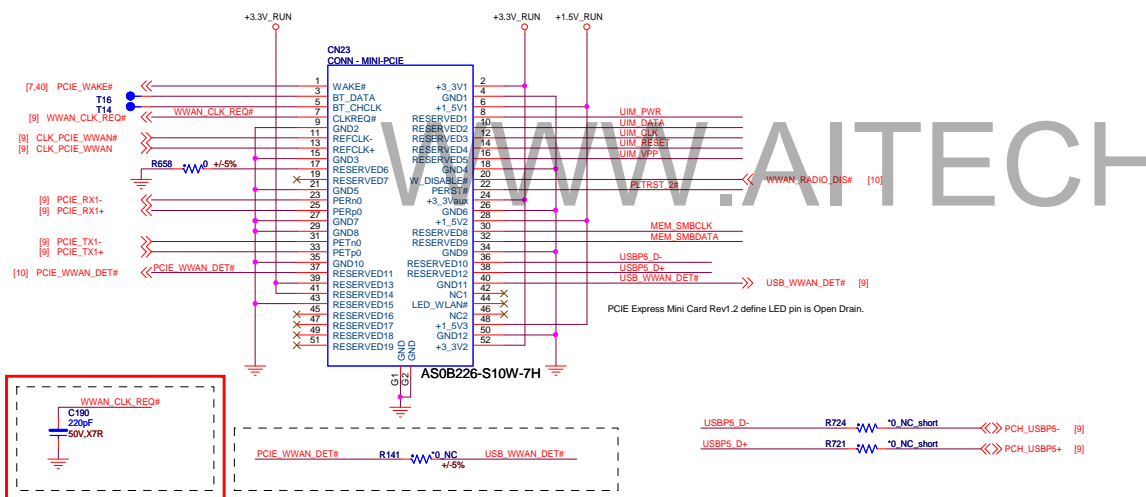
Mini DP



MiniCard WLAN connector



MiniCard WWAN connector

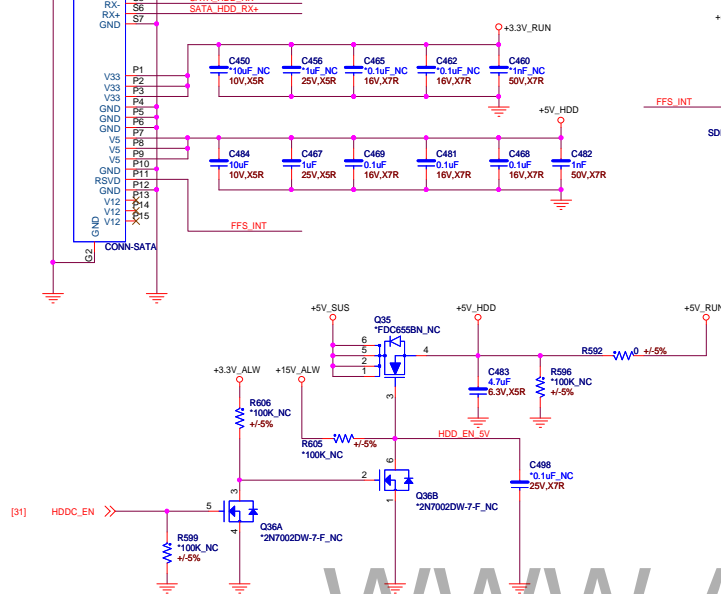
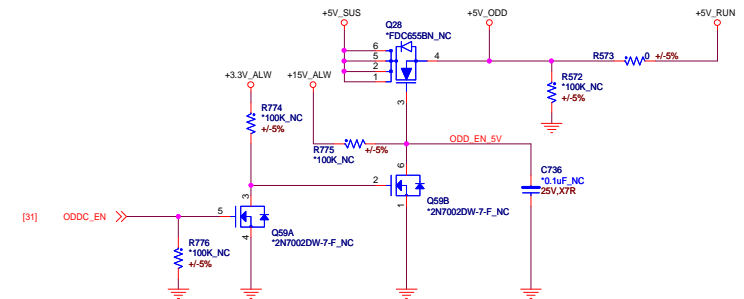


	MB Side		Module Side
Pin Name	Pin No.		Pin No.
GND	12	←→	1
MOD_DET	11	←→	2
COEX1_BT_ACTIVE	10	←→	3
BT_COEX_STATUS2	9	←→	4
BT_PRI_STATUS	8	←→	5
LINK_IND	7	←→	6
RADIO_DIS	6	←→	7
COEX2_WLAN_ACT	5	←→	8
VMAIN	4	←→	9
GND	3	←→	10
HUSB_DP	2	←→	11
HUSB_DP	1	←→	12

The schematic diagram illustrates the SATA controller interface. The SATA HDD signals (Tx+, Tx-, Rx-, Rx+, and GND) are connected to the controller pins P1 through P15. The controller is powered by +3.3V_RUN and +5V_HDD. The diagram includes capacitors C450 through C482 with their respective values and footprints.

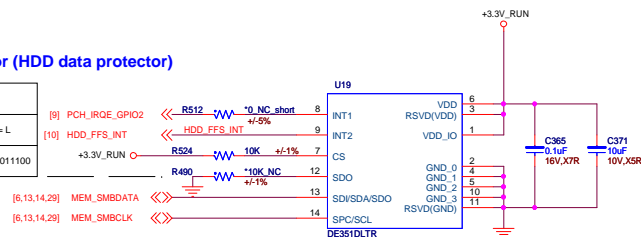
Capacitor Values and Footprints:

- C450: 10uF_NC 10V_XSR
- C456: 1uF_NC 25V_XSR
- C465: 0.1uF_NC 16V_X7R
- C462: 0.1uF_NC 16V_X7R
- C460: 1nF_NC 50V_X7R
- C484: 10uF_XSR
- C467: 1uF 25V_XSR
- C469: 0.1uF 16V_X7R
- C481: 0.1uF 16V_X7R
- C468: 0.1uF 16V_X7R
- C482: 1nF 50V_X7R

[illegible]

3-axis Fall Sensor (HDD data protector)

I2C Address Setting	
SDO = H	SDO = L
Addr = 0011101	Addr = 0011100



Re-Driver

PS8511_VDDb

R583 4.7k $\pm 5\%$

R586 4.7k $\text{NC} \pm 5\%$

R587 4.7k $\text{NC} \pm 5\%$

R582 0 $\text{NC} \pm 5\%$

R589 0 $\text{NC} \pm 5\%$

R584 0 $\text{NC} \pm 5\%$

R585 0 $\text{NC} \pm 5\%$

R588 0 $\text{NC} \pm 5\%$

VDD : 60 ~ 95 mA

PS8511_VDDb

C444 0.1uF 10V X5R

C464 10nF 25V X7R

For PS8511B: VDD = 3.3V

FB21 120 ohm, 200mA

FB20 120 ohm, 200mA, NC

1 2 $\rightarrow +3.3V_RUN$

1 2 $\rightarrow +1.5V_RUN$

U34

PS8511ATQFN20GTR

1 A_INp

2 A_INn

3 GND

4 B_OUTp

5 B_OUTn

6 VDD

7 EN

8 A_PRES

9 A_BSTp

10 A_BSTn

11 B_INp

12 GND#13

13 A_OUTp

14 A_OUTn

15 SATA_HDD TX+ C

16 SATA_HDD TX- C

17 SATA_HDD RX- C

18 SATA_HDD RX+ C

19 SATA_HDD TX+ C

20 SATA_HDD TX- C

21 SATA_HDD RX- C

22 SATA_HDD RX+ C

PS8511BTFQFN20GTR-A3

1 2 $\rightarrow +3.3V_RUN$

R575 0 $\text{NC} \pm 5\%$

R576 0 $\text{NC} \pm 5\%$

R577 4.7k $\text{NC} \pm 5\%$

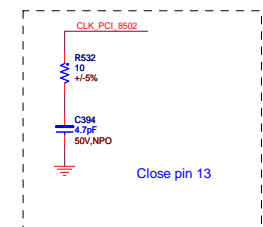
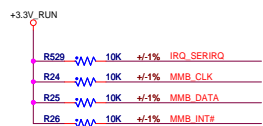
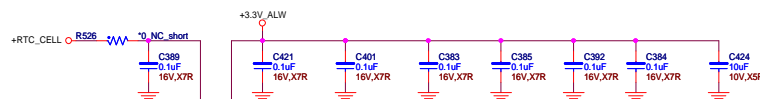
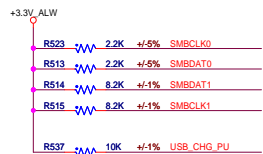
R578 4.7k $\text{NC} \pm 5\%$

PS8511_VDDb

DE : PS8511ATQFN20GTR

75LVC412ARTJR

Note
1. PARADE : PS8511ATQFN20GTR
2. TI : SN75LVCP412ARTJR



- [2,6,9,16] PLTRST_1#
[9] CLK_PCI_8502
[8,29] LPC_LAD0
[8,29] LPC_LAD1
[8,29] LPC_LAD2
[8,29] LPC_LAD3
[8,29] LPC_LFRAME#
[24] FP_BACK_EN
[7] CLKRUN#
[8] IRQ_SERIRQ
[10] SIO_EXT_SMI#
[10] SIO_EXT_SCI#
[10] SIO_A20GATE
[10] SIO_RCN#
[26] LCD_BAK

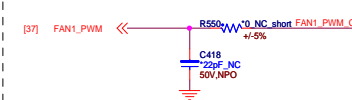
- CLK_PCI_8502
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_LFRAME#
FP_BACK_EN
CLKRUN#
IRQ_SERIRQ
SIO_EXT_SMI#
SIO_EXT_SCI#
SIO_A20GATE
SIO_RCN#
LCD_BAK

- PCH_EC_SPL_CS#
PCH_EC_SPL_CLK
PCH_EC_SPL_SO
PCH_EC_SPL_SI
EC_FLASH_SPL_CS#
EC_FLASH_SPL_DIN
EC_FLASH_SPL_DO
EC_FLASH_SPL_CLK

- KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
KSO16
KSO17
KSO18
KSO19
KSO20
KSO21
KSO22
KSO23
KSO24
KSO25
KSO26
KSO27
KSO28
KSO29
KSO30
KSO31
KSO32
KSO33
KSO34
KSO35
KSO36
KSO37

IT8502E

Reserve for RF/EMC



IT8512/02NX

POWER

GPIO

LPC

PWM

CLOCK

A/D

D/A

HSPI

SPI

PS/2

SM BUS

KBMX

GND

AC_PRESENT

BAT_A_LED

BAT_B_LED

ME_FWP

LID_SW#

ACAV_IN

ODDC_EN

AUD_NS_MUTE#

ALUION

IMVP_VR_ON

MAIN_PWR_SW#

SIO_SLP_S3#

USB_CHG_DET#

SUS_ON

PCH_PWRGD

USB_BACK_EN#

USB_CHG_EN

LCD_TST

PW_SUT_LED#

PWM_VADJ

USB_SIDE_EN#

LED_WLAN_MMS

KB_BACKLITE_EN

BEEP

FAN1_TACH

CR1_CD1_S01_CD#

SIO_RUN_ON

IMVP_PWRGD

INT_CCD#

CRIT_TEMP_REP#

MMS_INT#

HWP#

PBAT_PRES#

IIMP

SIO_SLP_S5#

PS_ID

SKT0CC#

PCH_RSMRST#

SIO_PWRST#

SUS_PWR_ACK

TOUCH_PAD_LED#

GPU_RST#

AUX_ON

GPU_PWR_ON

CLK_TP_SIO

CAP_LED

SMBCLK0

SMBCLK1

SMBCLK2

SMBCLK3

SMBCLK4

SMBCLK5

SMBCLK6

SMBCLK7

SMBCLK8

SMBCLK9

SMBCLK10

SMBCLK11

SMBCLK12

SMBCLK13

SMBCLK14

SMBCLK15

SMBCLK16

SMBCLK17

SMBCLK18

SMBCLK19

SMBCLK20

SMBCLK21

SMBCLK22

SMBCLK23

SMBCLK24

SMBCLK25

SMBCLK26

SMBCLK27

SMBCLK28

SMBCLK29

SMBCLK30

SMBCLK31

SMBCLK32

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SMBCLK35

SMBCLK36

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SMBCLK39

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SMBCLK41

SMBCLK42

SMBCLK43

SMBCLK44

SMBCLK45

SMBCLK46

SMBCLK47

SMBCLK48

SMBCLK49

SMBCLK50

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SMBCLK52

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SMBCLK57

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SMBCLK61

SMBCLK62

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SMBCLK68

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SMBCLK77

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SMBCLK83

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SMBCLK86

SMBCLK87

SMBCLK88

SMBCLK89

SMBCLK90

SMBCLK91

SMBCLK92

SMBCLK93

SMBCLK94

SMBCLK95

SMBCLK96

SMBCLK97

SMBCLK98

SMBCLK99

SMBCLK100

SMBCLK101

SMBCLK102

SMBCLK103

SMBCLK104

SMBCLK105

SMBCLK106

SMBCLK107

SMBCLK108

SMBCLK109

SMBCLK110

SMBCLK111

SMBCLK112

SMBCLK113

SMBCLK114

SMBCLK115

SMBCLK116

SMBCLK117

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SMBCLK145

SMBCLK146

SMBCLK147

SMBCLK148

SMBCLK149

SMBCLK150

SMBCLK151

SMBCLK152

SMBCLK153

SMBCLK154

SMBCLK155

SMBCLK156

SMBCLK157

SMBCLK158

SMBCLK159

SMBCLK160

SMBCLK161

SMBCLK162

SMBCLK163

SMBCLK164

SMBCLK165

SMBCLK166

SMBCLK167

SMBCLK168

SMBCLK169

SMBCLK170

SMBCLK171

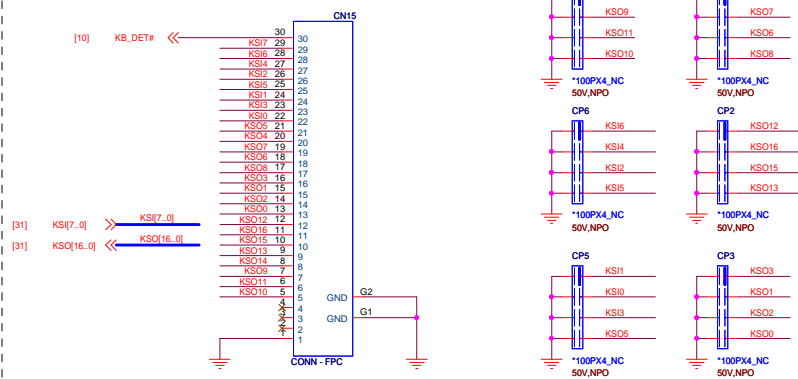
SMBCLK172

SMBCLK173

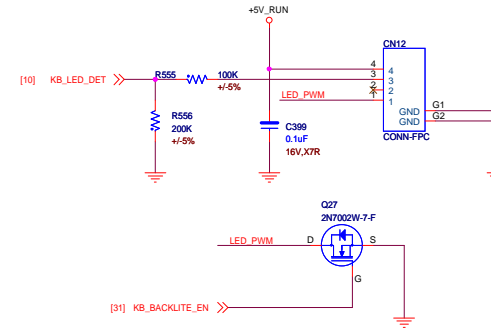
SMBCLK174

SMBCLK175

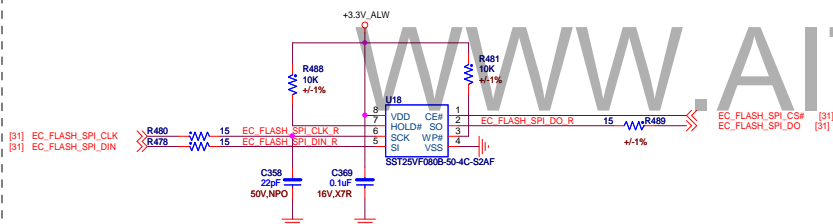
Keyboard connect



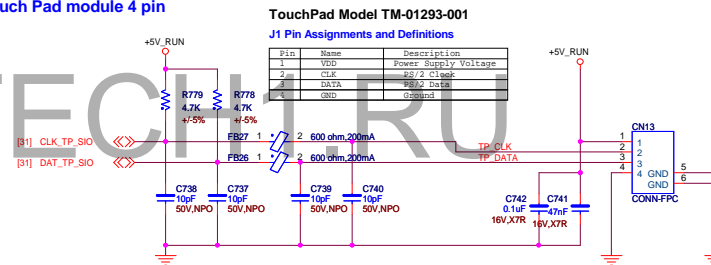
BACKLITE CONNECT



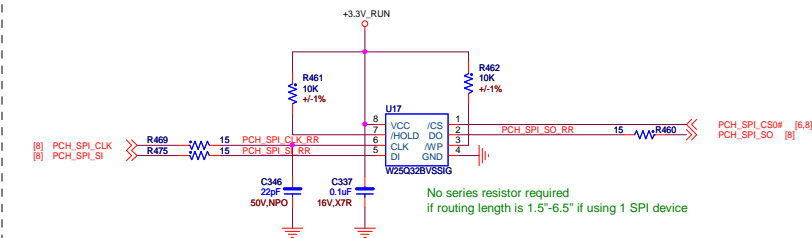
EC SPI ROM, (1M Byte)



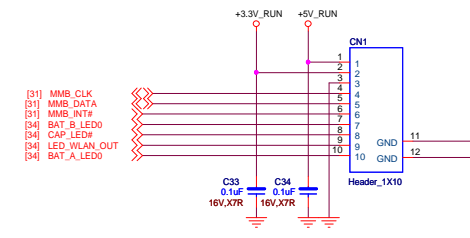
Touch Pad module 4 pin



PCH SPI ROM, (4M Byte)



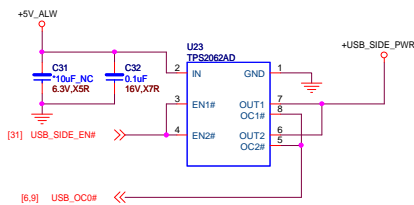
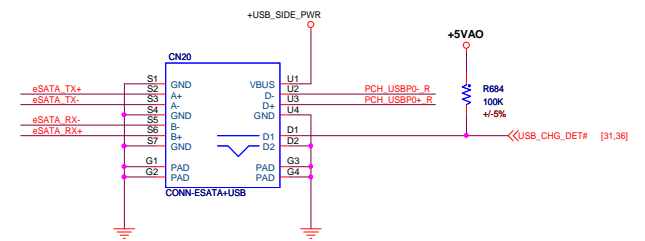
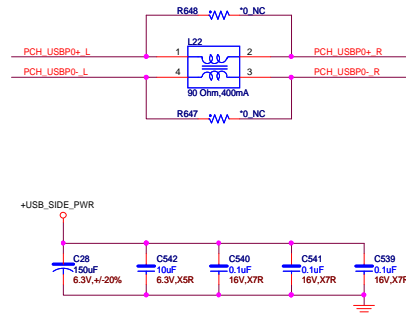
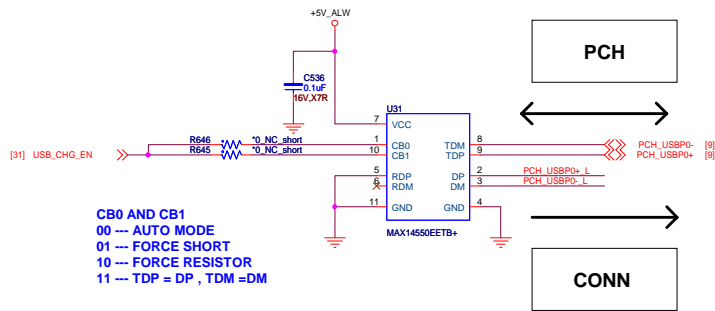
MMB module 10 pin



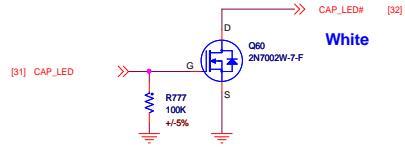
SATA Re-Driver(Removed Per EA has passed w/o re-driver)



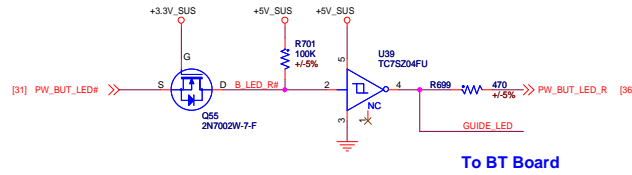
WWW.AITECH1.RU eSATA + USB Charge Conn



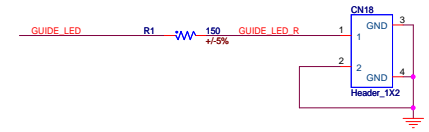
MMB \ CAP



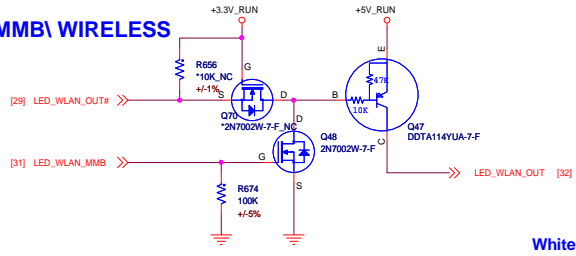
POWER \ BUTTON



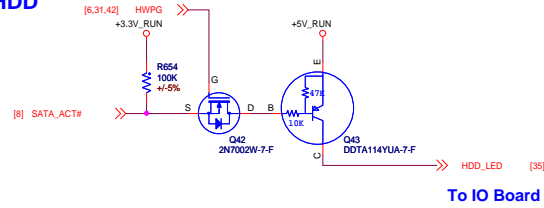
LIGHT GUIDE LED



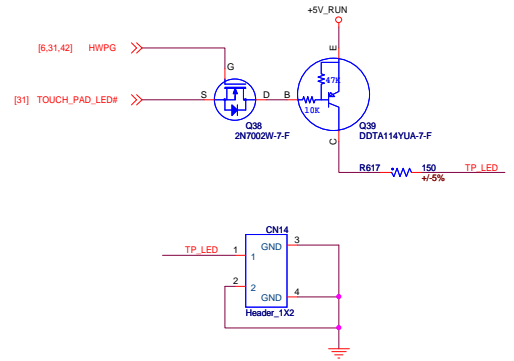
MMB \ WIRELESS



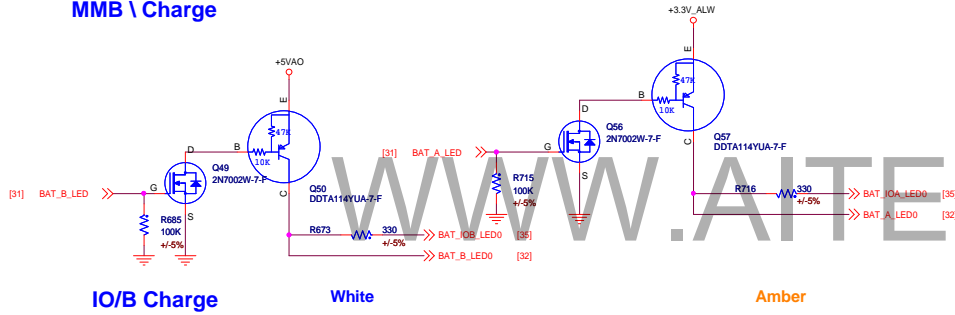
HDD



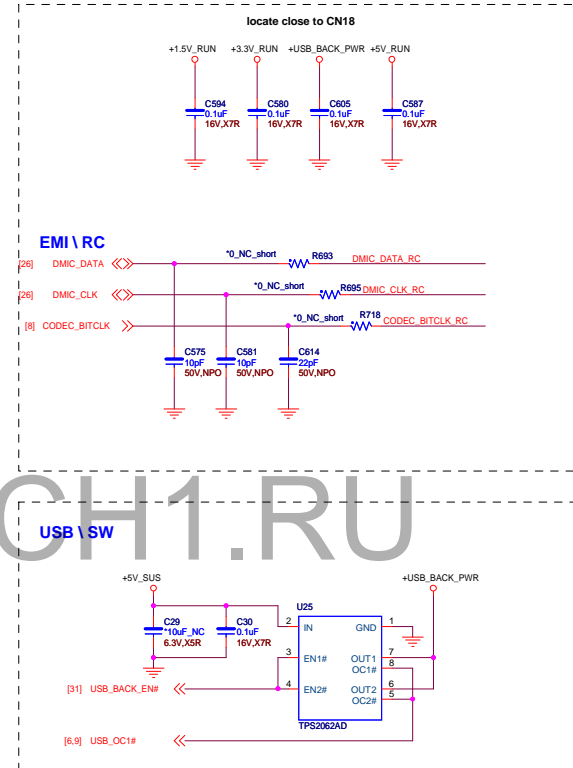
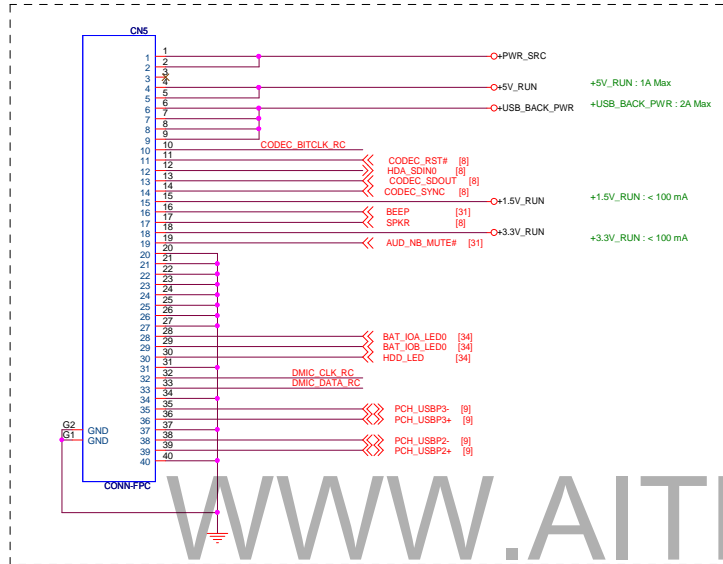
Touch Pad LED

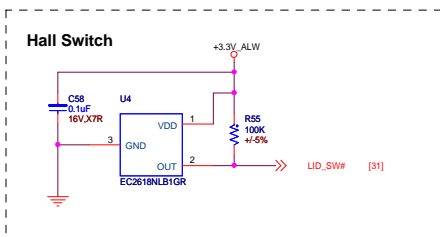


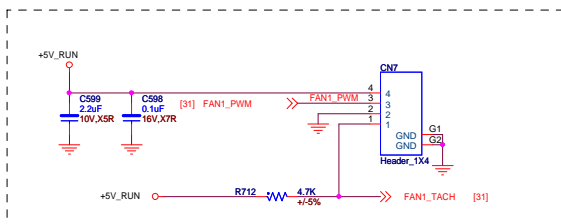
MMB \ Charge



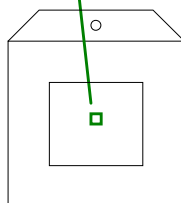
IO Board Conn



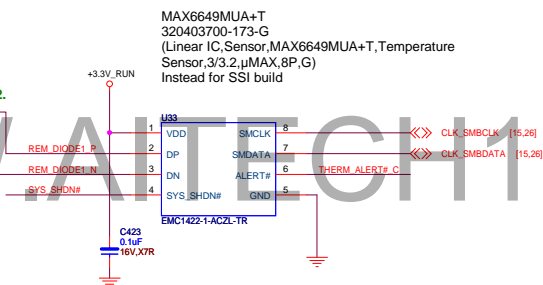




Place center on CPU Socket
at the same layer (OTP)



CAP close to
EMC1422 PIN#2.

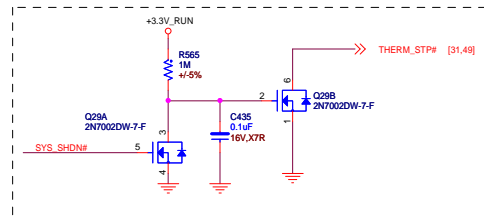


OTP 90 degree C



OTP degree table

SYS_SHDN#	10k ohm
THERM_ALERT#_C	
6.8k ohm	90 degree



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37 -- FAN, THERMAL

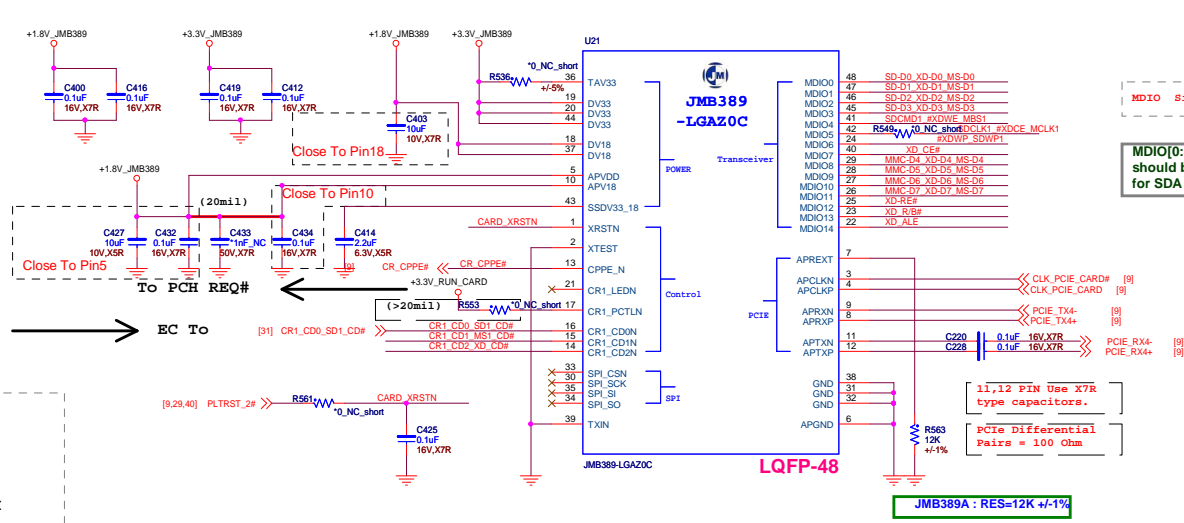
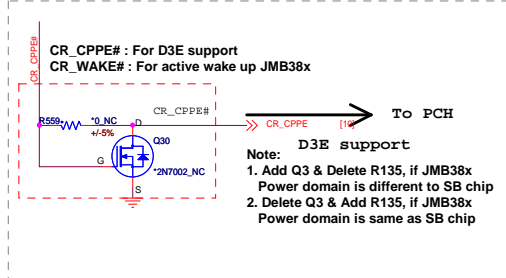
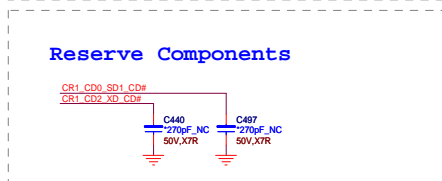
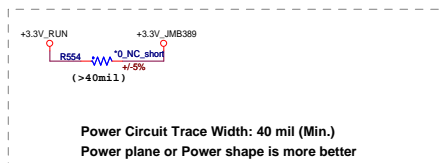
Document Number
Nichols 14"

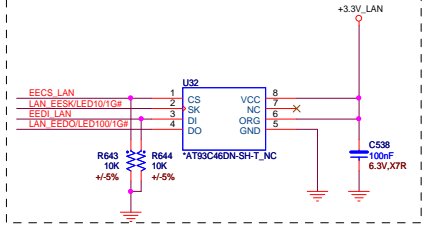
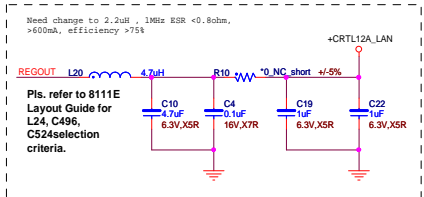
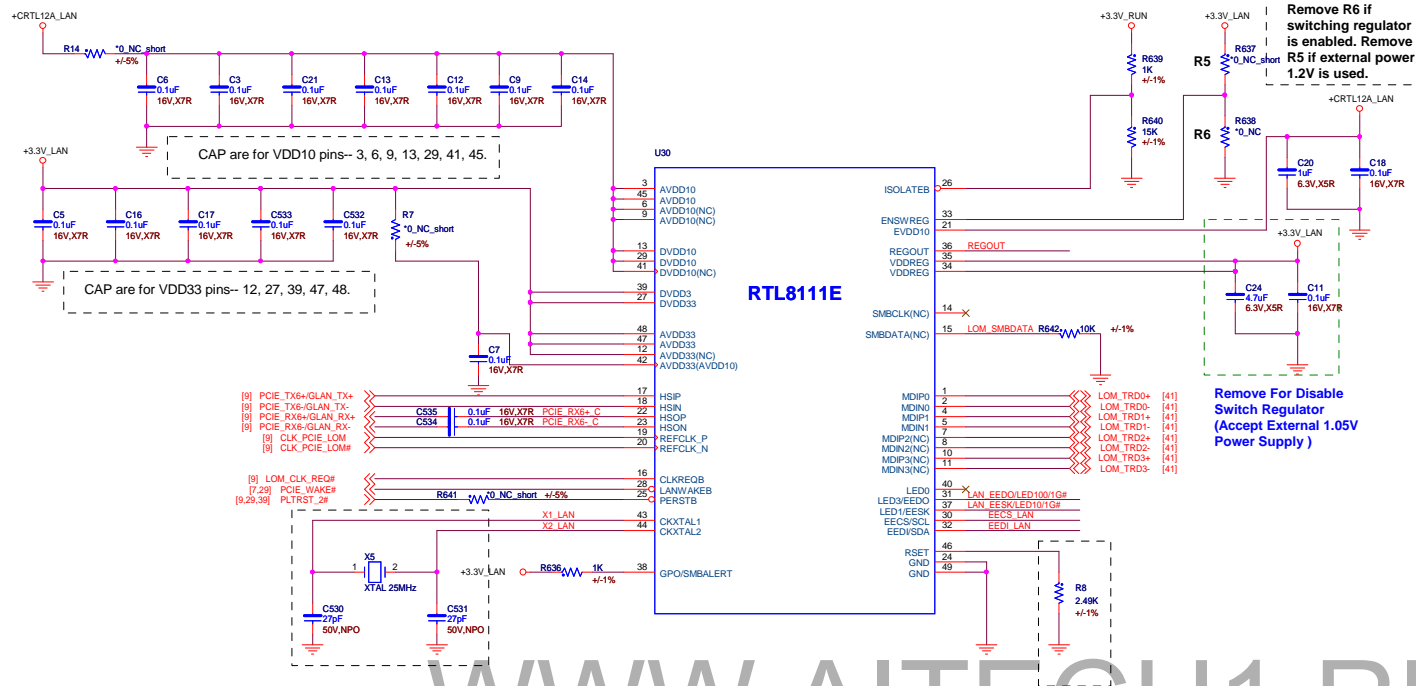
Date: Friday, August 20, 2010

Sheet 37 of 59

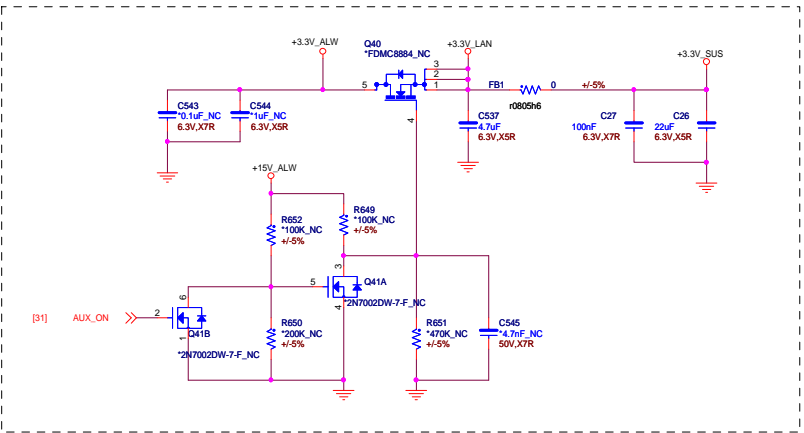
Rev
1A

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Power domain chart		
VDD33	3.3V	Digital
DVDD12	1.05V	Digital
AVDD12	1.05V	Analog
EVDD12	1.05V	Analog
AVDD33	3.3V	Analog



Transformer

The diagram illustrates the LFE9249-R Transformer, a component used in the LFE9249-R board. It shows the internal structure of the transformer, including the core, windings, and the connection points for the primary and secondary windings. The diagram is divided into two main sections: the primary winding (L21) and the secondary winding (L22).

Primary Winding (L21):

- Pin 1: TCT0
- Pin 2: TD0+
- Pin 3: TD0-
- Pin 4: TCT1
- Pin 5: TD1+
- Pin 6: TD1-
- Pin 7: TCT2
- Pin 8: TD2+
- Pin 9: TD2-
- Pin 10: TCT3
- Pin 11: TD3+
- Pin 12: TD3-

Secondary Winding (L22):

- Pin 24: TXCT3
- Pin 23: RJ45-TX3+
- Pin 22: RJ45-TX3-
- Pin 21: TXCT1
- Pin 20: RJ45-TX1+
- Pin 19: RJ45-TX1-
- Pin 18: TXCT2
- Pin 17: RJ45-TX2+
- Pin 16: RJ45-TX2-
- Pin 15: TXCT0
- Pin 14: RJ45-TX0+
- Pin 13: RJ45-TX0-

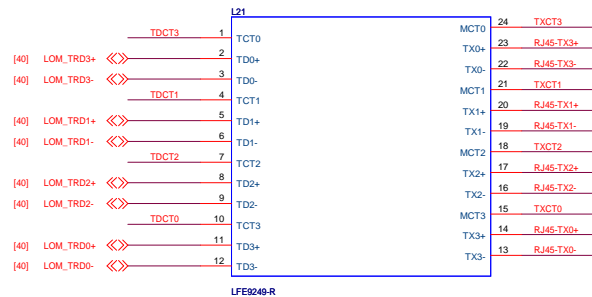
Internal Components:

- TDCT3
- TDCT1
- TDCT2
- TDCT0

Pin Connections:

- Pin 40: LOM_TRD3+ (connected to TDCT3)
- Pin 40: LOM_TRD3- (connected to TDCT1)
- Pin 40: LOM_TRD1+ (connected to TDCT1)
- Pin 40: LOM_TRD1- (connected to TDCT2)
- Pin 40: LOM_TRD2+ (connected to TDCT0)
- Pin 40: LOM_TRD2- (connected to TDCT0)
- Pin 40: LOM_TRD0+ (connected to TDCT0)
- Pin 40: LOM_TRD0- (connected to TDCT0)

Transformer Model: LFE9249-R



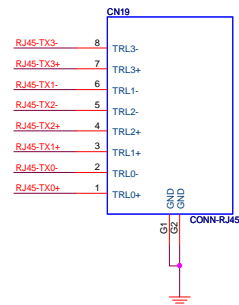
RJ45

RJ-45 Connector

The diagram illustrates the pin connections for an RJ-45 connector. A blue rectangular box represents the connector, with pins numbered 1 through 8 on the left side. The connections are as follows:

- Pin 8: **TRL3-** (red line)
- Pin 7: **TRL3+** (red line)
- Pin 6: **TRL1-** (red line)
- Pin 5: **TRL2-** (red line)
- Pin 4: **TRL2+** (red line)
- Pin 3: **TRL1+** (red line)
- Pin 2: **TRL0-** (red line)
- Pin 1: **TRL0+** (red line)

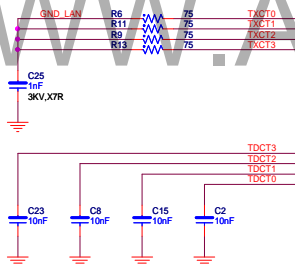
Below the connector box, a vertical line represents the cable. The cable is labeled **CONN-RJ45** and has a **GROUND** symbol at the bottom. The cable is connected to the **TRL0-** pin (pin 2) and the **TRL0+** pin (pin 1).

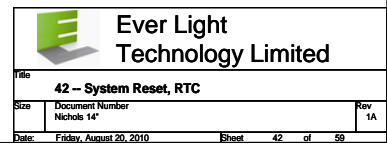
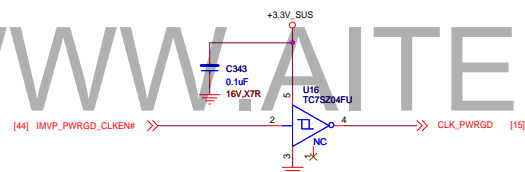
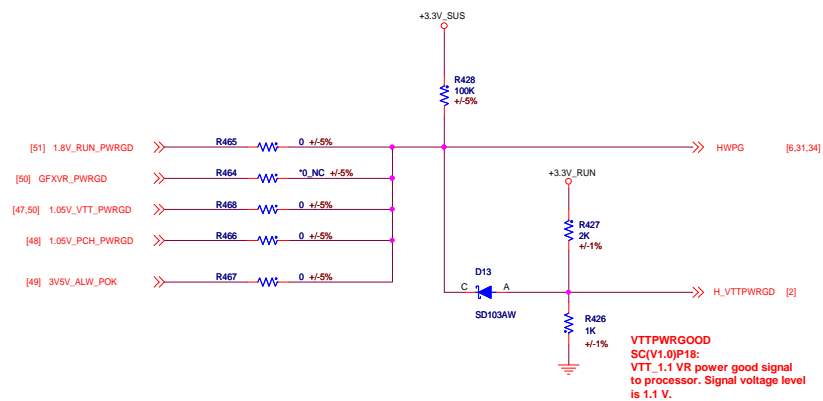


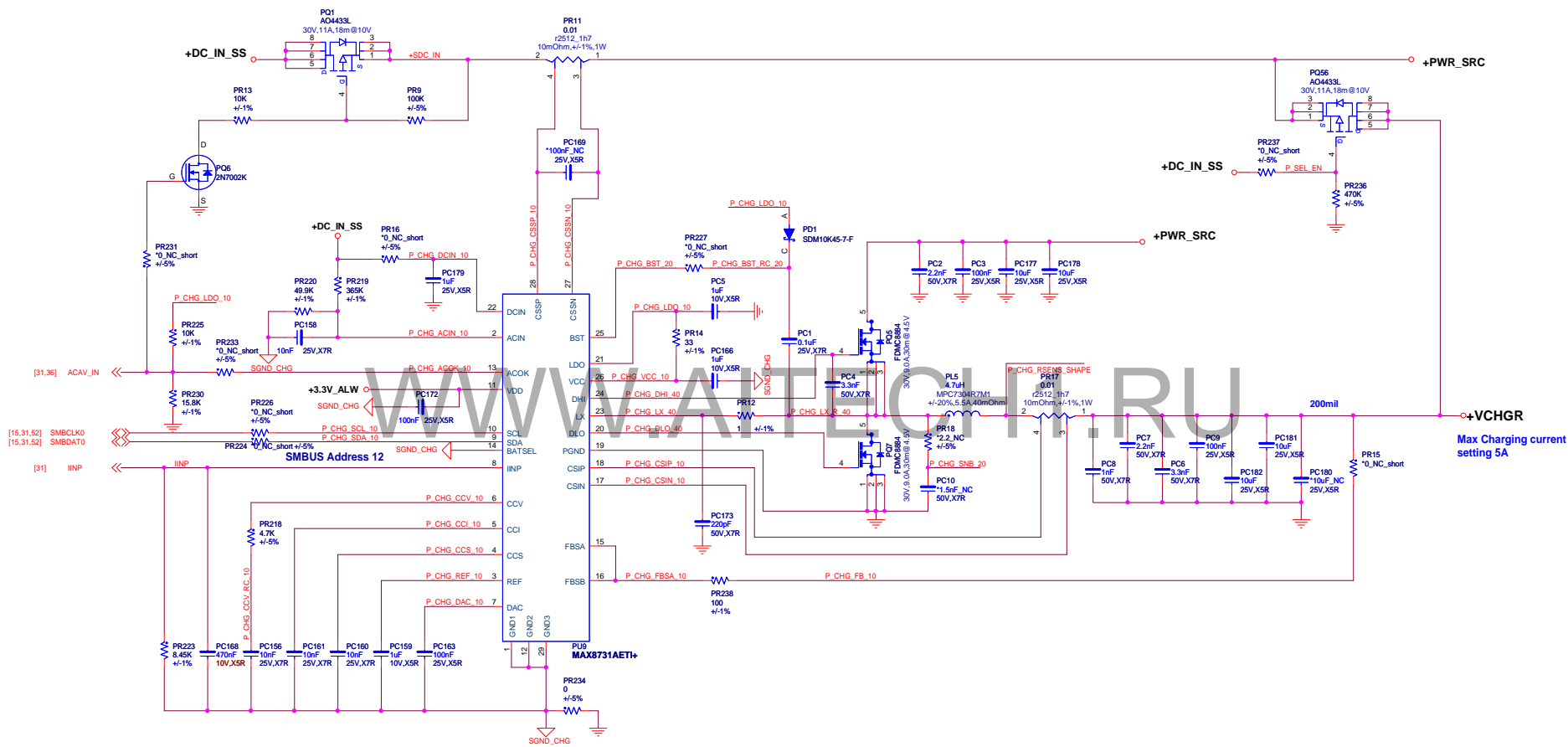
Reserved EMI

The diagram shows the following components and connections:

- Resistors:** R6, R11, R9, and R13 are 1k resistors connected in parallel between GND and LAN.
- Capacitor:** C25 is a 1nF capacitor connected between GND and 3KV_X7R.
- Capacitors:** C23 (10nF), C8 (10nF), C15 (10nF), and C2 (10nF) are connected between GND and various signal lines.
- Signal Lines:** TXD70, TXE11, TXE12, TXE13, TDCT3, TDCT2, TDCT1, and TDCT0.



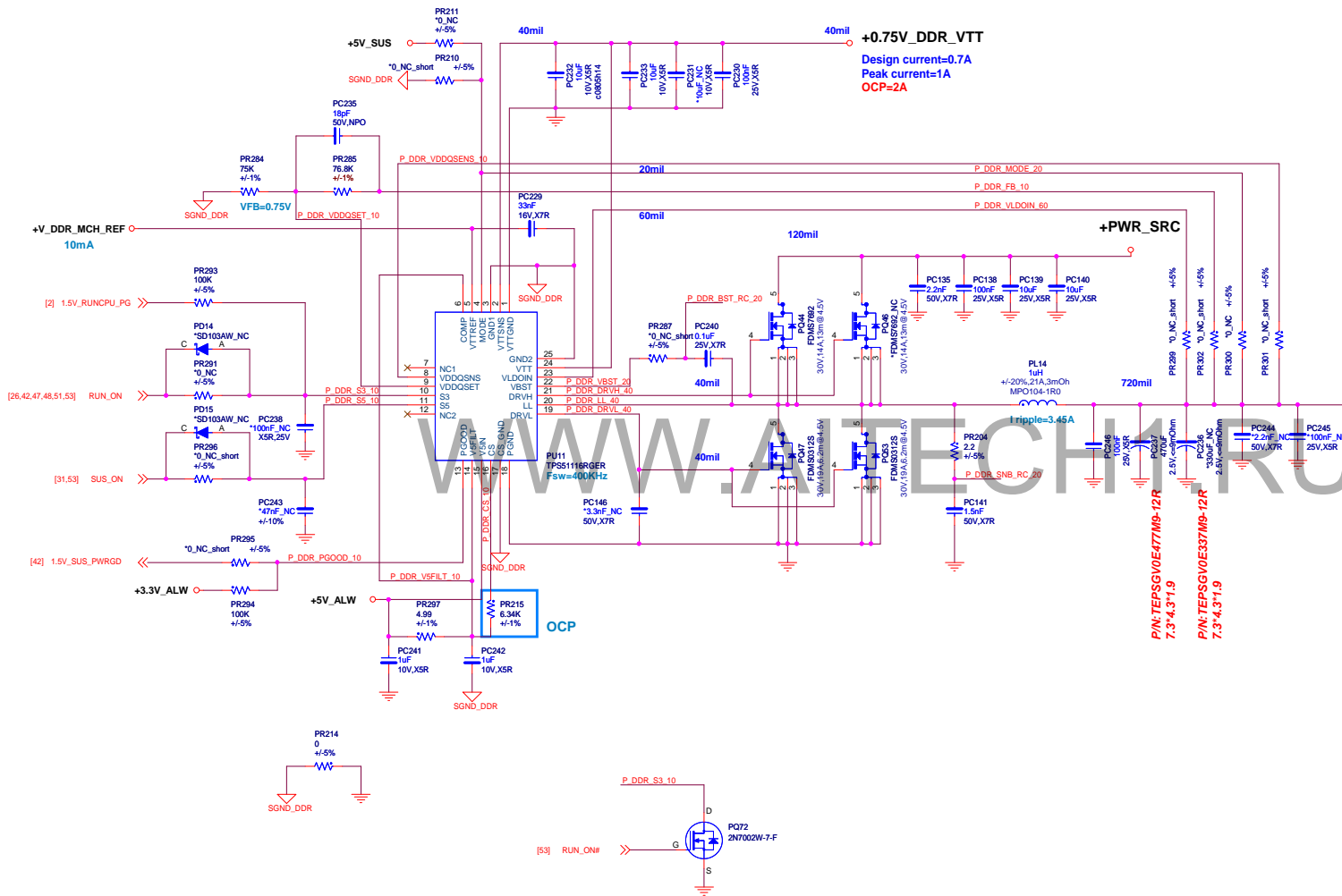




The OCP & slew rate value need to fine tune
Currently setup OCP=62.4A and S/R=6.2mV/uS



+1.5V_SUS & +0.75V_DDR_VTT POWER SUPPLY



Power stage

DDR III:

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.73A$$

2. Ripple Current:

$$I_{rip} = 3.45A$$

3. Ripple Voltage:

$$ESR / f = 9m\Omega$$

$$V = 31.05mV$$

4. Inductor Spec:

$$I_{sat} = 30A$$

$$I_{dc} = 21A$$

$$DCR = 2.8m\Omega (Typ)$$

5. MOSFET Spec:

$$H\text{-side MOSFET: FDM57692}$$

$$R_{ds(ON)} = 9.5m\Omega (Typ) \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 14A \quad (T = 25^\circ C)$$

$$I_{peak} = 50A \quad (Pulse Width < 300\mu s)$$

$$L\text{-side MOSFET: FDM50312S}$$

$$R_{ds(ON)} = 6.2m\Omega (Max) \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 19A \quad (T = 25^\circ C)$$

$$I_{peak} = 90A \quad (Pulse Width < 300\mu s)$$

Controller

DDR III:

1. Voltage & Current:

$$+1.5V: 1.5V / 16.8A$$

$$+0.75V: 0.75V / 1A$$

2. Frequency:

$$F = 400KHz$$

3. OCP:

$$Set PR144 = 6.81K\Omega$$

$$I_{ocp} = R_{ocp} \cdot 10uA / R_{ds(on)} + 1/2 \cdot I_{ripple}$$

$$I_{ocp} = 23.6A$$

4. Soft start time:

$$The Soft Start duration is 0.645ms$$

5. Inrush Current:

$$C_{total} = 470uF$$

$$I_{inrush} = C \cdot V_{out} / SS_time$$

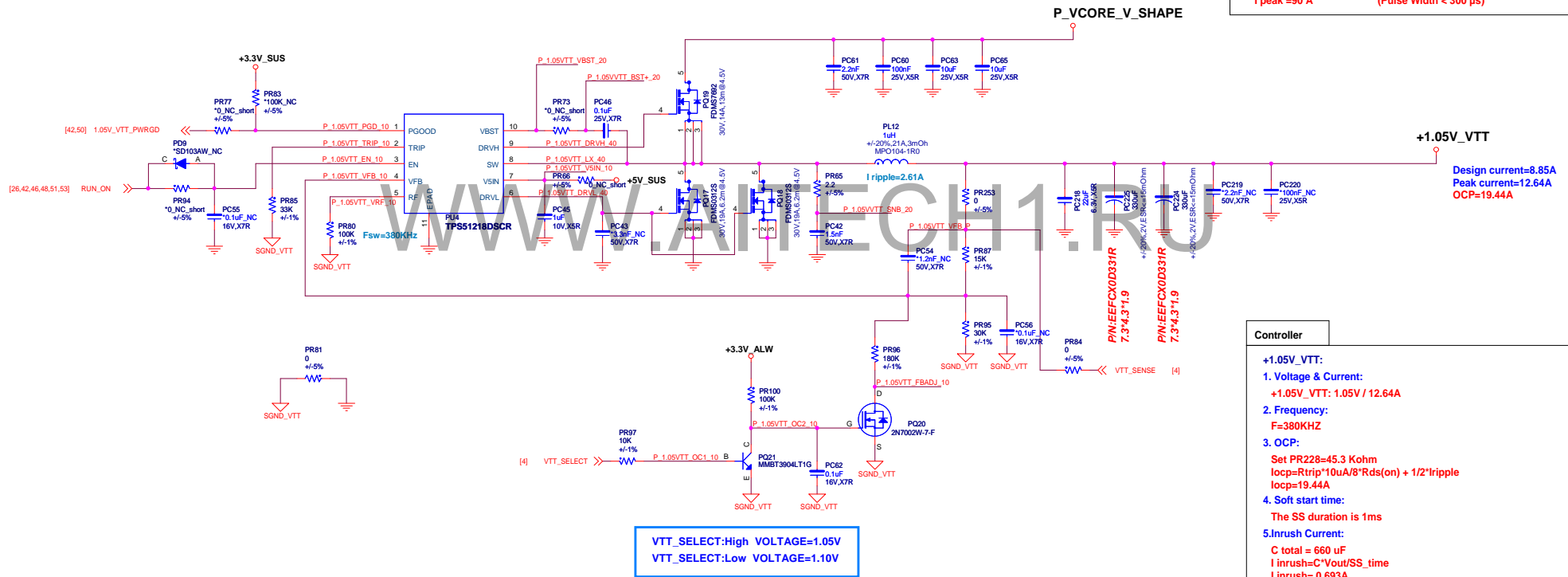
$$I_{inrush} = 1.093A$$

<Variant Name>

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Title			46 - 1.5V_SUS, 0.75V_DDR_VTT
Size	Document Number	Nichols 14". SW_ARD_Eric Ho	
Date	Friday, August 20, 2010	Sheet	46 of 59

+1.05V_VTT POWER SUPPLY



Power stage

+1.05V_VTT:

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.97A$$

2. Ripple Current:

$$I_{rip} = 2.61A$$

3. Ripple Voltage:

$$ESR/2 = 7.5m\Omega$$

$$V = 19.575mV$$

4. Inductor Spec:

$$I_{sat} = 30A$$

$$I_{dc} = 21A$$

$$DCR = 2.8m\Omega$$

5. MOSFET Spec:

H-side MOSFET: FDM57692

$$R_{ds(ON)} = 9.5m\Omega (TYP) \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 14A \quad (T = 25^\circ C)$$

$$I_{peak} = 50A \quad (Pulse Width < 300\mu s)$$

L-side MOSFET: FDM50312S

$$R_{ds(ON)} = 6.2m\Omega (Max) \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 19A \quad (T = 25^\circ C)$$

$$I_{peak} = 90A \quad (Pulse Width < 300\mu s)$$

Controller

+1.05V_VTT:

1. Voltage & Current:

$$+1.05V_VTT: 1.05V / 12.64A$$

2. Frequency:

$$F = 380KHz$$

3. OCP:

$$\text{Set } PR228 = 45.3K\Omega$$

$$I_{ocp} = R_{trip} \cdot I_o / (8 \cdot R_{ds(on)} + 1/2 \cdot I_{ripple})$$

$$I_{ocp} = 19.44A$$

4. Soft start time:

$$\text{The SS duration is 1ms}$$

5. Inrush Current:

$$C_{total} = 660\mu F$$

$$I_{inrush} = C \cdot V_{out} / SS_time$$

$$I_{inrush} = 0.693A$$

<Variant Name>

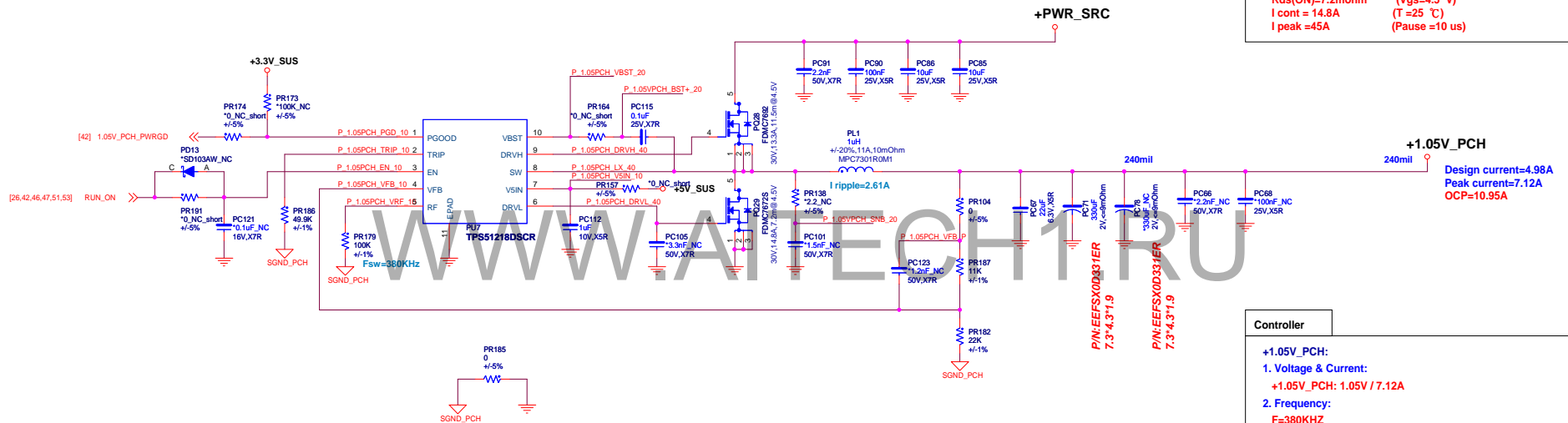
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Technology Limited

47 - PW_+1.05V_VTT(TPS51218)

Nichols 14" SW_ARD_Eric Ho

Date: Friday, August 20, 2010 Sheet 47 of 59

+1.05V_PCH POWER SUPPLY



Power stage

- +1.05V_PCH:**
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.11A$
 - Ripple Current:**
 $I_{rip} = 2.61A$
 - Ripple Voltage:**
 $ESR/1 = 9mohm$
 $V = 23.49mV$
 - Inductor Spec:**
 $I_{sat} = 23A$
 $I_{dc} = 11A$
 $DCR = 8mohm$
 - MOSFET Spec:**
H-side MOSFET: FDMC7692
 $R_{ds(ON)} = 11.5mohm$ ($V_{gs} = 4.5V$)
 $I_{cont} = 13.3A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause = 10 us)
L-side MOSFET: FDMC7672S
 $R_{ds(ON)} = 7.2mohm$ ($V_{gs} = 4.5V$)
 $I_{cont} = 14.8A$ ($T = 25^\circ C$)
 $I_{peak} = 45A$ (Pause = 10 us)

Controller

- +1.05V_PCH:**
- Voltage & Current:**
 $+1.05V_PCH: 1.05V / 7.12A$
 - Frequency:**
 $F = 380KHZ$
 - OCP:**
 Set PR184=56Kohm
 $I_{ocp} = R_{trip} \cdot I_o / (8 \cdot R_{ds(on)} + 1/2 \cdot I_{rip})$
 $I_{ocp} = 10.95A$
 - Soft start time:**
 The SS duration is 1ms
 - Inrush Current:**
 $C_{total} = 330uF$
 $I_{inrush} = C \cdot V_{out} / SS_time$
 $I_{inrush} = 0.3465A$

<Variant Name>

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48 -- PW_+1.05V_PCH(TPS51218)

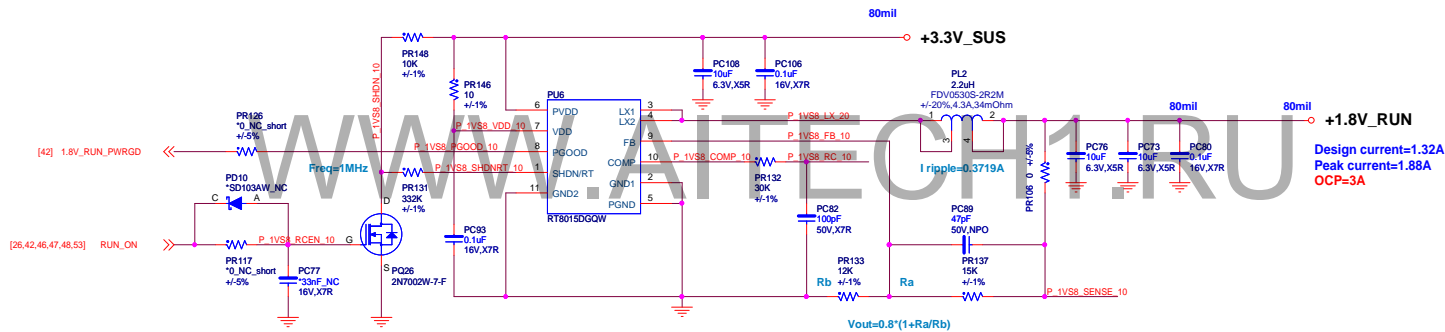
Size Document Number
Nichols 14" SW_ARD_Eric Ho

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+5V_ALW:	+3.3V_ALW:
1./P Current:	1./P Current:
$I_{in}=Vo/Io(0.75*Vin)=4.22A$	$I_{in}=Vo/Io(0.75*Vin)=3.08A$
2. Ripple Current:	2.Ripple Current:
$I_{rip}=2.79A$	$I_{rip}=2.75A$
3. Ripple Voltage:	3.Ripple Voltage:
$ESR/I=15mohm$	$ESR/I=15mohm$
$V=41.85mV$	$V=41.25mV$
4. Inductor Spec:	4.Inductor Spec:
$I_{sat}=9.8A$	$I_{sat}=9.8A$
$I_{dc}=9A$	$I_{dc}=9A$
$DCR=10.1mohm$	$DCR=10.1mohm$
5.MOSFET Spec:	
H-side MOSFET: AON614AL	
$R_{ds(ON)}=30mohm$	$(V_{gs}=4.5 V)$
$I_{cont} = 13A$	$(T = 25^{\circ}C)$
$I_{peak} = 27A$	$(Pause = 10 us)$

<p>+5V_ALW:</p> <p>1. Voltage & Current:</p> <p>+5V_ALW: 5V / 5.7A</p> <p>2. Frequency:</p> <p>F=400KHZ</p> <p>3. OCP:</p> <p>Set PR203=75 Kohm lcp=5uA*Rocp/10*Rds(on) lcp=8.77A</p> <p>4. Soft start time:</p> <p>The Soft Start duration is 1ms</p> <p>5.Inrush Current:</p> <p>C total = 220 uF I inrush=C*Vout/SS_time I inrush= 1.1A</p>	<p>+3.3V_ALW:</p> <p>1.Voltage&Current:</p> <p>+3.3V_ALW: 3.3V / 6.3A</p> <p>2.Frequency:</p> <p>F=300KHZ</p> <p>3.OCP:</p> <p>Set PR211=82KOhm lcp=5uA*Rocp/10*Rds(on) lcp=9.7A</p> <p>4.Inrush Current:</p> <p>C total = 220 uF I inrush=C*Vout/SS_time I inrush= 0.726A</p>
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+1.8V_RUN POWER SUPPLY

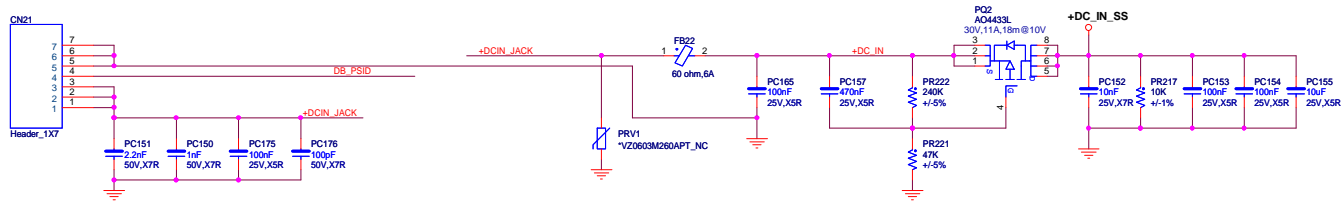
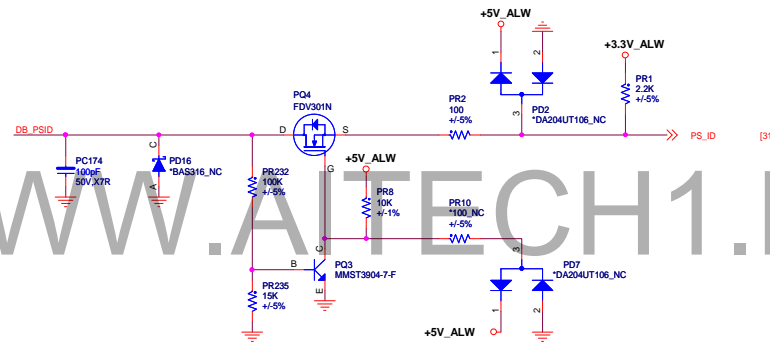
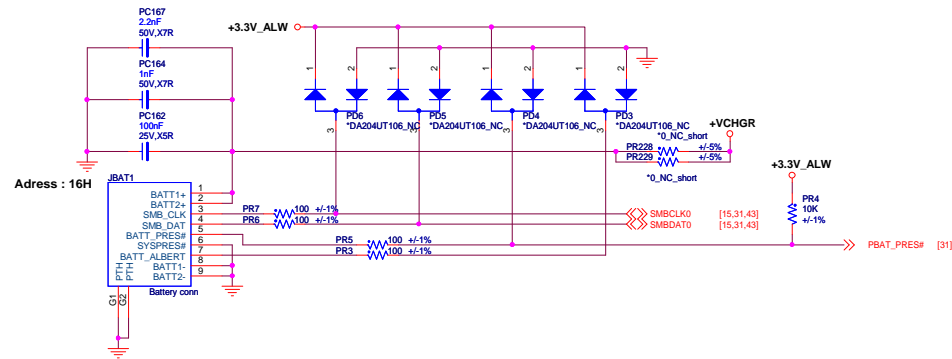


+1.8V_RUN @ 2A

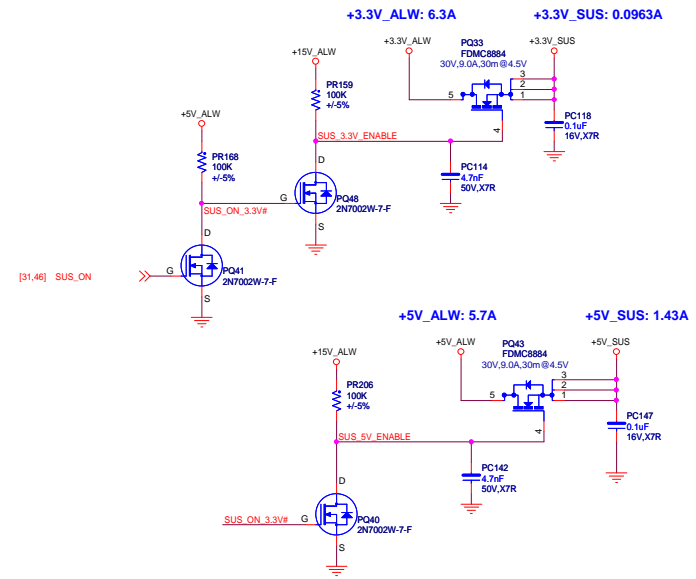
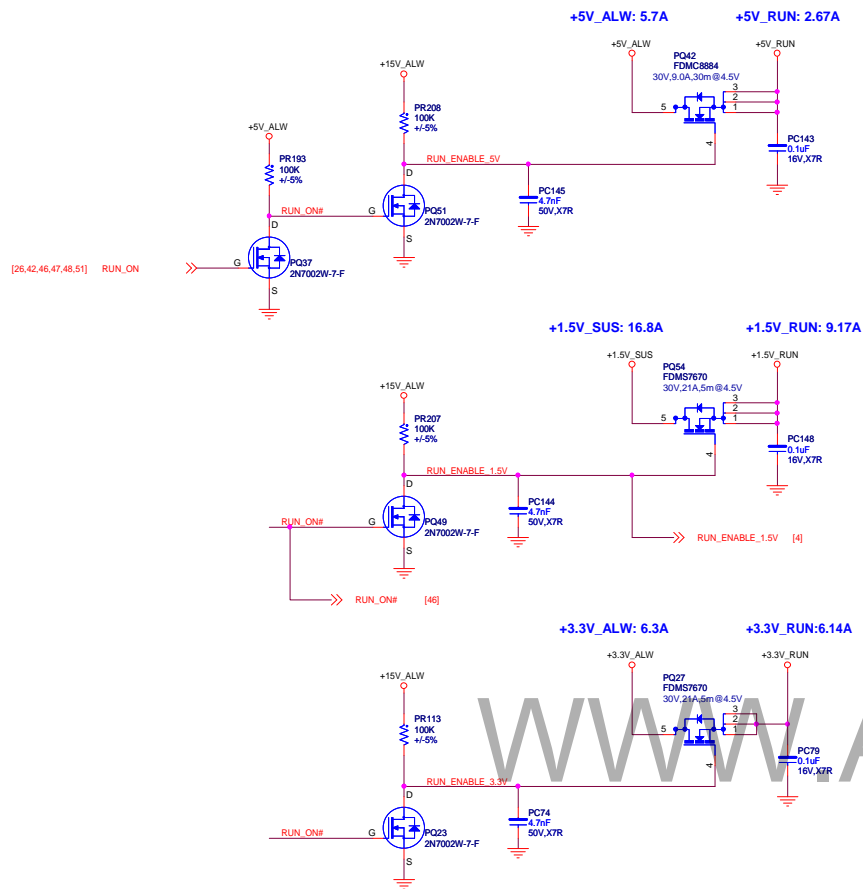
1. Supply Voltage:
 $V_{IN} = 3.3V$ (2.6V ~ 5.5V)
2. Supply Voltage:
 $V_{OUT} = 1.8V / 2A$
3. Current Limit:
 $I_{limit} = 3.2A(min)/3.8A(Typ)$
4. Continue Current:
 $I_{cont} = 2A$
5. Feedback Voltage:
 $V_{FB} = 0.8V$
6. Switching Frequency:
 $R_{rt} = 332 \text{ Kohm}$
 $F_{sw} = 1000 \text{ KHz}$

<Variant Name>

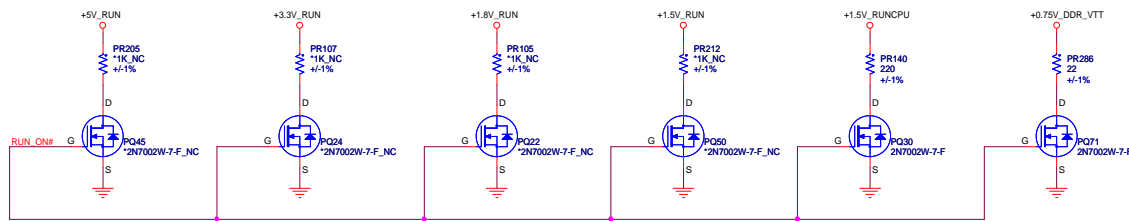
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51 - PW_SW_+1.8V(RT8015B)		
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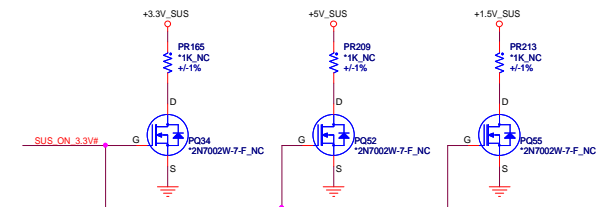
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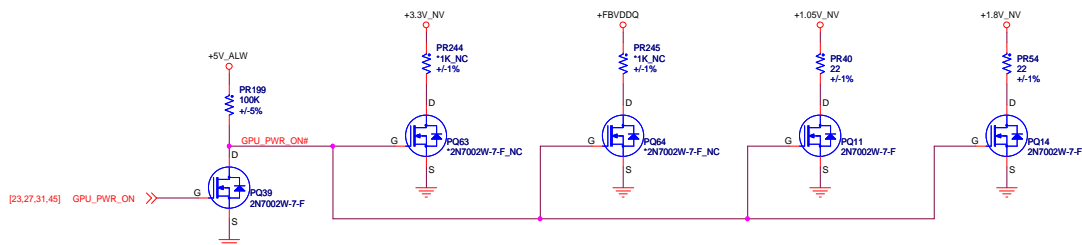
Reserve discharge path



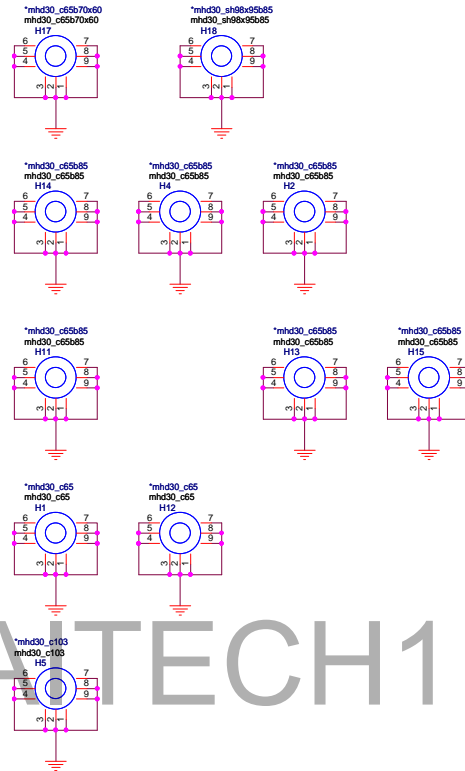
Reserve discharge path



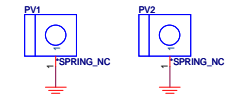
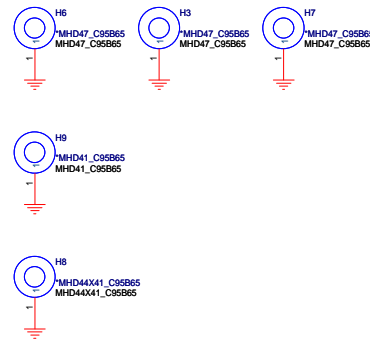
Reserve discharge path for NVDD



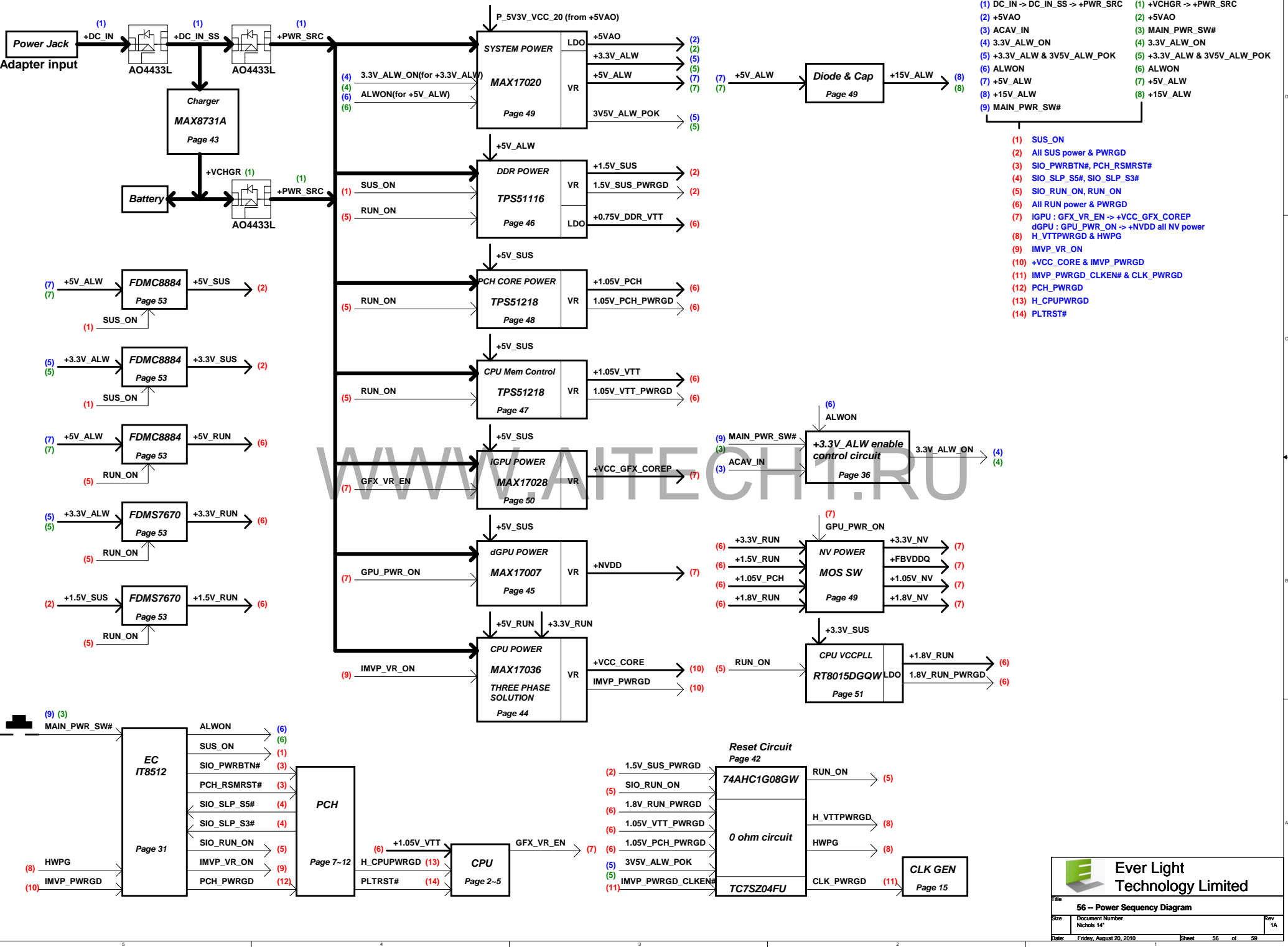
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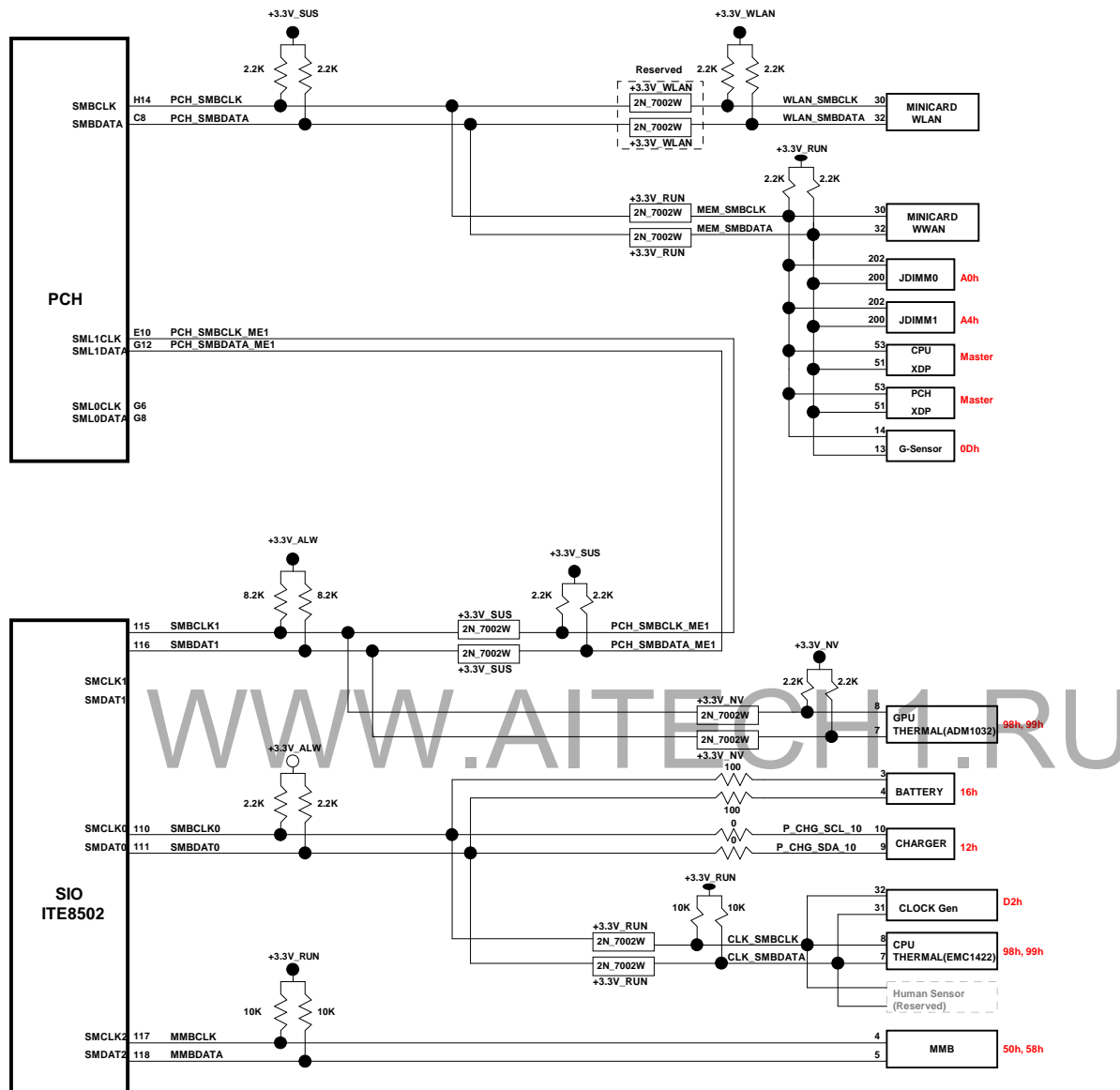


WWW.AITECH1.RU

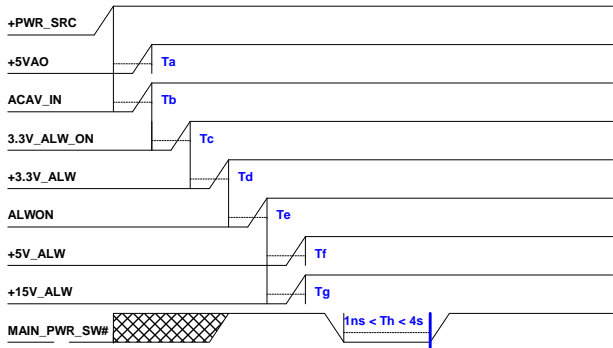


Nichols Power Design Block Diagram 2010/07/29

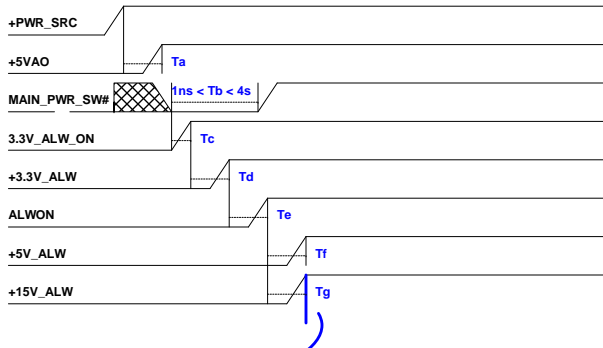




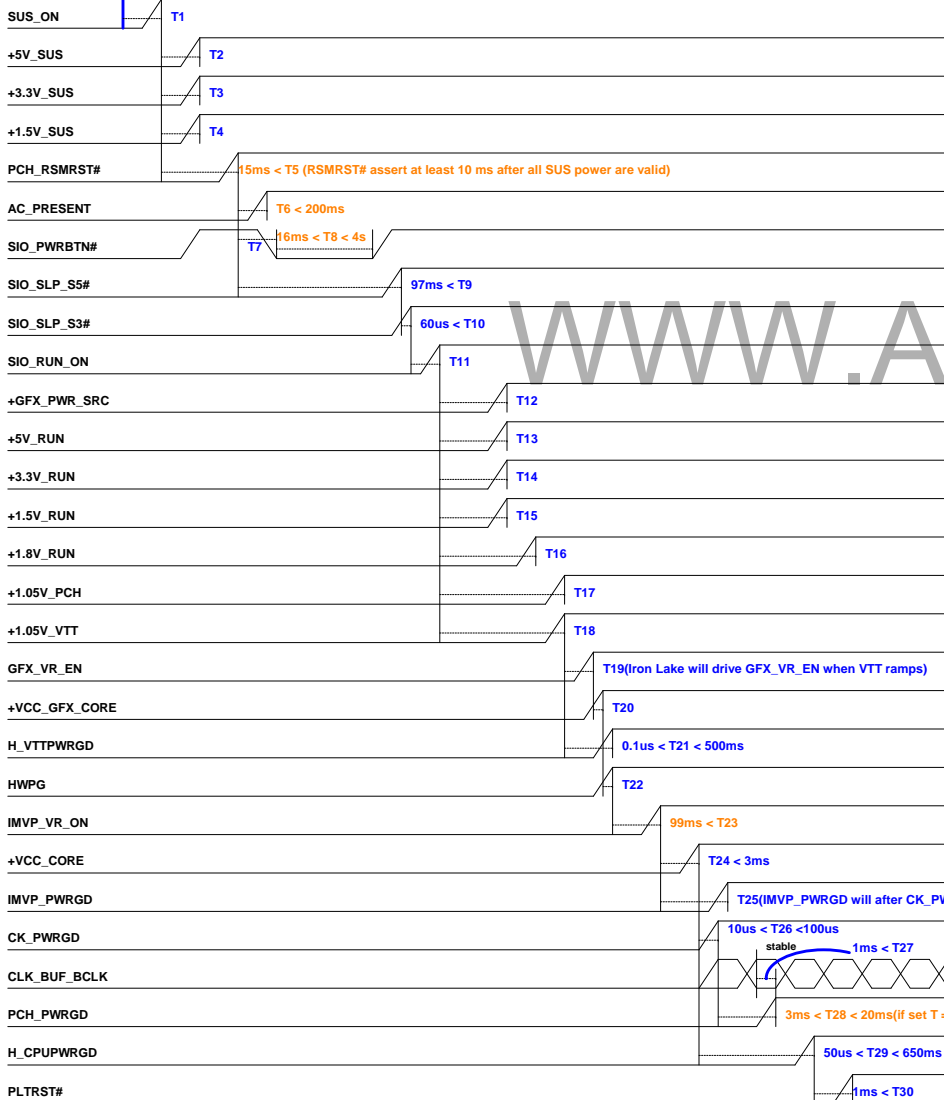
[AC with USB charge]



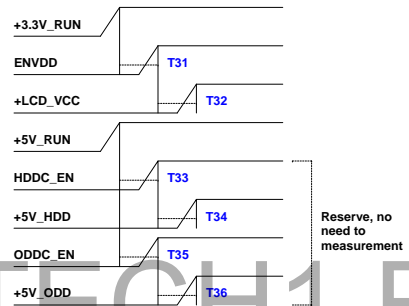
[Battery without USB charge]



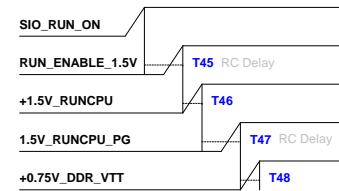
EC pay attention timing



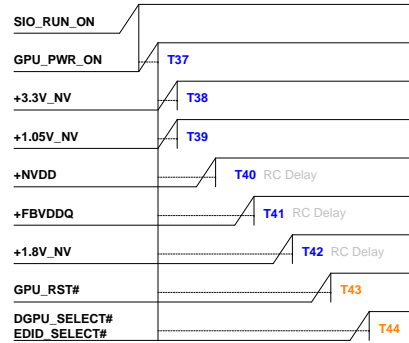
[LCD, HDD and ODD Power Sequence]



[W/ S3 Power Reduction DDR3 Sequence]



[GPU Power Sequence]




The ramp up time for any rail must be more than 40us.

+NVDD <= +3.3V_NV + 0.5V

+FBVDDQ <= +3.3V_NV + 0.5V

GPU_RST# must de-asserted after all power rails reach within it's spec.

DGPU_SELECT# and EDID_SELECT# must get set after GPU_RST#

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
MBB	1	49	7/14				+3.3V_ALW current will over OCP design point.	Change PR188 to 100kohms.
	2	22	7/14				Change FB23 from DCR 100m ohms to 50m ohms per NV recommend.	Done.
	3	31	7/14				Change BID to ST2 stage setting.	Change R545 to 33Kohms.
	4	10	7/14				WWAN card cannot be recognized when system wake up from S3.	Change WWAN_RADIO_DIS# PCH GPIO from GPIO15 to GPIO35.Delete R437.
	5	26	7/20				Change N-Trig digitizer power plan from RUN to SUS for supporting fast wake up feature.	NC R808 and pop R809.
	6		7/26				SMT request	Change L1,L4,L6,L22,L23 footprint from cks0805h11 to cks0805h13.
	7	10,26	7/27				Solve GPIO glitch issue	Change P26 net USB_OC2# to LPM#,R796 0 ohm change to 100 ohm,P10 GPIO15 change to LPM#
	8	08,31	7/27				Change by PUR request	Change X4,Y1 PN to 710104400-310-G,footprint to x4s69x14h14
	9		7/28				Remove 0ohm resistor for ST2 stage	Modify as excel file"Nichols_0 ohm removal list(ST2)_0728_Scott"
	10	55	7/28				Modify screw hole type for MP	Change H17,H18,H14,H4,H2,H11,H13,H15,H1,H12,H5 footprint.
	11	18,19	7/29				Layout request	Change VRAM U1,U2,U5,U10,U37,U38,U41,U43 footprint to fbga96gh12_MBB
	12	56	7/29				Power diagram update	Change P56 for power diagram update
	13	49,46	7/30				Power fine tune OCP resistors value	Change PR188 to 100K,PR178 to 68K,PR215 to 6.3K.
	14	34	8/2				Fine tune LED brightness	Change P699 330ohm to 470ohm
	15		8/3				PN category issue	Change C417,PC59,PC222, C746,PC71,PC78,PC187,PC188,PC193 PN from 62110DD00-024-G to 62120B000-024-G
	16	26	8/3				Fine tune N-TRIG resistor value	Change R796 tolerance from +/-5% to +/-1%.
	17	24	8/4				Fine tune HDMI_TX2+_BOUT/HDMI_TX2-_BOUT signal eyes.	Change R162 to 383ohm
	18	50	8/5				fine tune result of +VCC_GFX_COREP load line	Change R149 to 11Kohm
	19	26	8/16				Fine tune N-TRIG timing to meet SPEC(100ms)	Change GPIO15 to GPIO41
	20	31	8/16				BIOS setting strap for BID	Change R545 to 100Kohm
	21		8/20				Remove power portion 0 ohm for X-build	Modify as excel file"Nichols_0 ohm removal list(A00)_Scott"
								<div><div></div><div>Ever Light Technology Limited</div></div> <div><div><div>Title</div><div>59 – Change list-2</div></div><div><div>Size</div><div>Document Number</div><div>Nichols Discrete</div></div><div><div>Date:</div><div>Friday, August 20, 2010</div></div><div><div>Sheet</div><div>59</div><div>of</div><div>59</div></div><div><div>Rev</div><div>1A</div></div></div>